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APPLICATION NOTE

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Using M68HC11 Microcontrollers with WSI Programmable Peripheral Devices

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INTRODUCTION

Following system development using M68HC711 microcontroller (MCU) devices with EPROM or one time programmable ROM (OTPROM), a final design is often implemented using an equivalent mask-programmed M68HC11 device. However, there is a quick, cost-effective alternative to this method of going to production.

WSI manufactures a complete line of PSD programmable MCU peripherals that make it possible to use a ROM-less M68HC11 derivative instead of a mask-programmed device. PSD devices combine EPROM, SRAM, programmable logic for memory map decoding, programmable I/O ports, an address latch, power management, and other capabilities on a single chip. A “twin chip” solution can increase flexibility, provide expanded memory and enhanced I/O, lower power consumption, and lower cost — all with a minimum of software and hardware modifications.

This application note describes the process of converting from a prototype design that uses an M68HC711 device to a production design that uses a low-cost M68HC11 derivative and a WSI PSD.

CONVERSION PROCEDURES

There are eight steps in the conversion process. Each is discussed in detail in the following text.

1. Choose the M68HC11 and PSD
2. Add the PSD to the design
3. Configure the M68HC11 for expanded mode operation
4. Configure the PSD
5. Make memory map and I/O port selections
6. Modify M68HC11 code to address memory and I/O
7. Integrate M68HC11 code with PSD configuration data
8. Program the PSD

CHOOSE THE M68HC11 AND PSD

The M68HC11 family offers a wide range of operating voltage and frequency selections. **Table 1** shows M68HC11 Family devices, including M68L11 low-power devices, that can be used in two-chip systems. EPROM/OTPROM devices are shown in bold. WSI PSDs are available in a variety of configurations. PSDs provide a larger memory size, I/O port expansion, and programmable logic to an M68HC11 system. Low-power PSDs are a perfect complement to M68L11 MCUs.

Table 1 Motorola M68HC11 Devices

Motorola Part Number	ROM	RAM	EEPROM	I/O	A/D
MC68HC11A0 MC68L11A0	0	256	0	22	Yes
MC68HC11A1 MC68L11A1	0	256	512	22	
MC68HC11A7 MC68L11A7	8K	256	0	38	
MC68HC11A8 MC68L11A8	8K	256	512	38	
MC68HC11C0	0	256	0	35	Yes
MC68HC711D3	**4K**	**192**	**0**	**32**	**No**
MC68HC11D0	0	192	0	14	No
MC68HC11D3	4K	192	0	32	
MC68HC711E9	**12K**	**512**	**512**	**38**	**Yes**
MC68HC11E0 MC68L11E0	0	512	0	22	Yes
MC68HC11E1 MC68L11E1	0	512	512	22	
MC68HC11E8 MC68L11E8	12K	512	0	38	
MC68HC11E9 MC68L11E9	12K	512	512	38	
MC68HC711E20	**20K**	**768**	**512**	**38**	**Yes**
MC68HC11E20	20K	768	512	38	Yes
MC68HC811E2	0	256	2K	38	Yes
MC68HC11F1 MC68L11F1	0	1K	512	30	Yes
MC68HC711K4	**24K**	**768**	**640**	**62**	**Yes**
MC68HC11K0 MC68L11K0	0	768	0	37	Yes
MC68HC11K1 MC68L11K1	0	768	640	37	
MC68HC11K3 MC68L11K3	24K	768	0	62	
MC68HC11K4 MC68L11K4	24K	768	640	62	
MC68HC711L6	**16K**	**512**	**512**	**46**	**Yes**
MC68HC11L0 MC68L11L0	0	512	0	30	Yes
MC68HC11L1 MC68L11L1	0	512	512	30	
MC68HC11L5 MC68L11L5	16K	512	0	46	
MC68HC11L6 MC68L11L6	16K	512	512	46	
MC68HC711P2	**32K**	**1K**	**640**	**62**	**Yes**
MC68HC11P2	32K	1K	640	62	Yes

Table 2 shows PSD devices that are recommended for use with M68HC11 and M68L11 family members.

Table 2 Recommended Devices

Device	EPROM	RAM	I/O
PSD311C1	32K	—	19
PSD311	32K	2048	19
PSD411A1	32K	2048	40

Table 3 shows typical twin-chip alternatives to particular M68HC711 or M68L711 systems.

Table 3 Alternative System Configurations

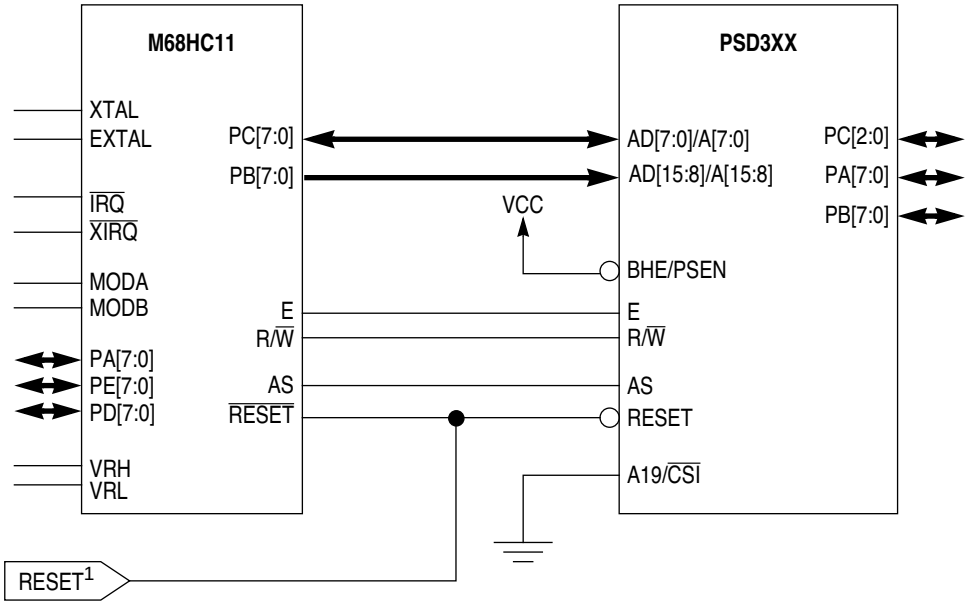
	Device	ROM	RAM	EEPROM	I/O	A/D
Single Chip	**MC68HC711D3**	**4K**	**192**	**0**	**32**	**No**
Twin Chip	MC68HC11D0 + PSD311C1	32K	192	0	33	No
Single Chip	**MC68HC711E9/20**	**12K/20K**	**512/768**	**512**	**38**	**Yes**
Twin Chip	MC68HC11A0/1 + PSD311C1	32K	256	0/512	41	Yes
Twin Chip	MC68HC11A0/1 + PSD311	32K	2304	0/512	41	Yes
Twin Chip	MC68HC11D0 + PSD311C1	32K	192	0	33	No
Twin Chip	MC68HC11E0/1 + PSD311C1	32K	512	0/512	41	Yes
Twin Chip	MC68HC11ED0 + PSD311C1	32K	512	0	33	No
Single Chip	**MC68HC11K4**	**24K**	**768**	**640**	**62**	**Yes**
Twin Chip	MC68HC11K0/1 + PSD411A1	32K	2816	0/640	77	Yes
Twin Chip	MC68HC11K0/1 + PSD311	32K	816	0/640	56	Yes
Single Chip	**MC68HC11L6**	**16K**	**512**	**512**	**46**	**Yes**
Twin Chip	MC68HC11L1 + PSD311C1	32K	512	0/512	49	Yes

ADD THE PSD TO THE DESIGN

Migration from an M68HC711 single-chip system to an M68HC11/PSD system can be accomplished in one of three ways.

1. By building a daughter board that plugs into the MCU socket on an existing printed circuit board. The board includes the M68HC11, the PSD, and system clock generation circuitry. Including the clock generator on the daughter board is important to minimize radiated EMI.
2. By placing an edge or row connector on an existing printed circuit board to allow access to a PSD device on a daughter board. The minimum signals needed include the address/data lines and control signals (R/$\overline{W}$, E, AS, $\overline{RESET}$). This requires changing the existing schematic.
3. By redesigning the existing printed circuit board to accommodate the PSD device.

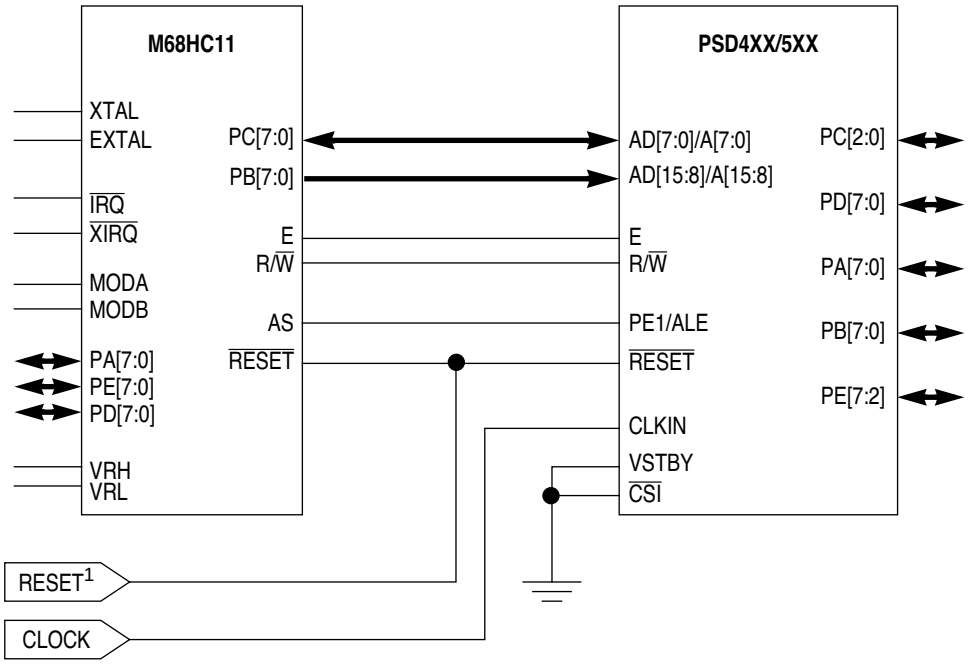
Figure 1 and **Figure 2** are examples of interfacing an M68HC11 to particular PSD devices. Please refer to the appropriate Motorola data book and to the WSI *PSD Design and Applications Handbook* for more information.



NOTES:
1. HC11 reset line must be pulled up to VDD.

HC11 PSD3 SCHEM

Figure 1 Typical M68HC11 and PSD3XX System



NOTES:
1. HC11 reset line must be pulled up to VDD.

HC11 PSD4/5 SCHEM

Figure 2 Typical M68HC11 and PSD4XX/5XX System

CONFIGURE THE M68HC11 FOR EXPANDED MODE OPERATION

M68HC11 operating mode is determined by the logic state of the MODA and MODB pins during system reset or power up. To configure the MCU for expanded mode operation, make the reset state of the MODA pin HIGH by pulling it up to VDD through a pullup resistor.

CONFIGURE THE PSD

PSD software must be used to configure the PSD. There are two different software packages available.

PSD-SILVER software supports the PSD3XX devices and includes the MAPLE and MAPPRO software modules which run under the DOS platform. MAPLE software is used to configure the PSD chip. It features simple menu driven commands for selecting different device configurations. It also provides mapping of the EPROM, SRAM, and chip select outputs into the user's address space, and locates the files to be programmed into the EPROM segments. MAPPRO enables the user to program PSDs on a WSI MagicPro III® programmer.

PSDsoft WS7001 or WS7002 software supports the PSD3XX, PSD4XX, and PSD5XX families and runs under MicroSoft® Windows® (PSD3XX support included in PSDsoft available Q295). It includes PSDabel, PSD configuration, PSD compiler, PSDsilos III simulator, and PSD programming software. The PSDsoft environment allows design and simulation of the on-chip PLD logic under Data I/O ABEL®, PSD interface selections to any MCU, configuration of the I/O, and address mapping of the EPROM and SRAM memory, among other things.

PSD-to-M68HC11 interface configuration is simple and straightforward. Configuration is performed by selecting certain option bits in the PSD software package. For MC68HC11A, C, D, E, and L devices, the PSD is configured for multiplexed mode. For MC68HC11F, K, and P devices, the PSD is configured for non-multiplexed mode. For all versions of the M68HC11, the other option bits on the PSD device are set as follows: R/$\overline{W}$ and E mode, active high AS (ALE), active low $\overline{RESET}$, and combined memory mode. To complete the configuration process, PSD Ports A and B must be configured as general-purpose I/O, to replace M68HC11 Ports B and C, which are used for address and data lines when the MCU is operating in expanded mode.

For a better understanding of the M68HC11 to PSD interface configuration information, please refer to the pin descriptions section of the appropriate Motorola data book and to Table 5 and Figure 12 in WSI Applications Note 011 for PSD3XX devices, and the section beginning with Figure 12 in Applications Note 029 for PSD4XX/5XX devices.

MAKE MEMORY MAP AND I/O PORT SELECTIONS

To convert from an M68HC711 system to a system that uses a ROM-less M68HC11 and a PSD, the content of the M68HC711 ROM must be transferred to PSD EPROM, and mapped externally. The default state of the ROMON bit in the CONFIG register of ROM-less M68HC11 devices is zero, so all accesses to the ROM address space automatically go external. Virtually no change in the MCU address map is required because PSD EPROM can be mapped anywhere on a block boundary using the address map menu in the PSD software.

For example, assume a PSD device with 32 Kbytes of EPROM is selected. The PSD311 has eight blocks of 4 Kbyte x 8 EPROM. Each block can be mapped on a 4-Kbyte block boundary in the address range as originally defined in the OTP application. The PSD411A1 has four blocks of 8 Kbyte x 8 EPROM, and each can be mapped to an 8-Kbyte block boundary. Please refer to the modes and memory section of the appropriate Motorola data book, to Figure 32 in WSI Applications Note 011 for the PSD3XX, and to Table 7 in WSI Applications Note 029 for the PSD4XX/PSD5XX devices.

For PSDs that include an additional 2 Kbyte x 8 SRAM, the SRAM can be mapped anywhere within the address space on a 2-Kbyte boundary to extend the SRAM already supplied on the M68HC11.

PSDs also offer from 19 to 40 configurable I/O pins that can replace I/O pins that are used for other purposes when the M68HC11 operates in expanded mode or enhance the function of the available ports. The programmable I/O is addressed via an offset from a base address that is selected in the PSD software. These

offsets are shown in Table 6 in the PSD3XX data sheets, Tables 21–23 in the PSD4XX data sheet, and in Tables 29–31 in the PSD5XX data sheet.

For example, the following steps must be performed to replace ports B and C on an M68HC711 with ports A and B on a PSD311 device.

1. Refer to the appropriate PSD data sheet to determine the correct offsets.
2. Set the CSIOPORT (CSP) base address of the PSD. The base address can be mapped to any boundary from 256 bytes to 2 Kbytes. In this example, the CSIOPORT base address starts at $2000.
3. Port B on the M68HC11 is mapped to port A on the PSD311. For compatibility with port B on the M68HC11, which is an output-only port, port A on the PSD311 is set for output. This is accomplished by writing $FF (output) to the PSD311 port A data direction register, located at $2004 (offset four from base address).
4. Port C on the M68HC11 is mapped to port B on the PSD311. The direction of the individual I/O pins in PSD311 port B is determined by the definition in the original OTP application. The direction is set by writing to $2005 (offset five from base address). To make a pin an input, the appropriate bit in the register must be cleared; to make a pin an output, the appropriate bit must be set.
5. To write data to PSD311 port A and port B pins, the data must be written to $2006 for port A and to $2007 for port B. Data from the PSD311 port A and port B pins must be read from $2002 and $2003, respectively.

Other M68HC11 resources, such as EEPROM, SRAM, vectors, and the control registers are mapped internally and do not require any memory map redirection.

MODIFY M68HC11 CODE TO ADDRESS PSD MEMORY AND I/O

Change M68HC11 I/O port addresses to match the port address at the appropriate offset from the specified PSD I/O port base address (CSIOPORT).

INTEGRATE M68HC711 CODE WITH PSD CONFIGURATION DATA

Code that would normally be programmed into M68HC711 EPROM must be merged with PSD configuration information to create one output file. This is done during the compile procedure in the PSD software. The single output file is then downloaded to an industry-standard programmer (or the WSI MagicPro III PC-compatible programmer) and used to program the PSD device.

PROGRAM THE PSD

The output file (filename.obj) generated from the PSD software compiler is now ready to be programmed into a device from one of the three PSD families (PSD3XX, PSD4XX, or PSD5XX). A list of programmer manufacturers that support the PSD devices can be obtained from a WSI sales office or sales representatives. Programmers which support the PSD devices are available from Data I/O, BP Microsystems, and Logical Devices.

CONCLUSION

A single-chip Motorola M68HC711 control system can be quickly and easily converted to a system that uses a ROM-less M68HC11 and a WSI Programmable MCU peripheral. A small investment in hardware and software modification can provide an increase in system memory, expanded I/O, lower power consumption, greater design flexibility, and lower cost.

NOTES

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