

# Motorola Semiconductor Application Note

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## AN1705

### Noise Reduction Techniques for Microcontroller-Based Systems

By Imad Kobeissi

#### Introduction

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With today's advancements in semiconductor technology and the push toward faster microcontroller units (MCUs) and peripherals, new product designs are faced with an increasing threat from electromagnetic interference (EMI).

Earlier, the issue of emission and interference was referred to as EMI or RFI (for radio frequency interference). It is now referred to in more positive terms by replacing "interference" with "compatibility." Electromagnetic compatibility (EMC) encompasses both emission and susceptibility for a given system. Although this application note focuses primarily on emission, some of the guidelines presented throughout this document will affect susceptibility as well.

EMI can, and often does, cause delays in the product development schedule. Early and continuous attention to the effects of EMC/EMI will give the product the best possible chance for minimum cost and schedule delays, while lack of attention in this area will almost certainly translate to added cost and schedule delay.



Interference can be minimized if not completely eliminated. A system is electromagnetically compatible if it satisfies three criteria:

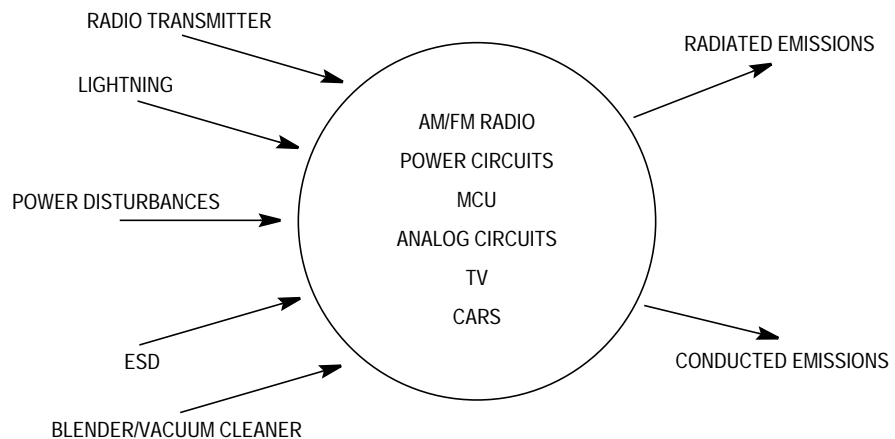
1. It does not cause interference with other systems.
2. It is not susceptible to emissions from other systems.
3. It does not cause interference with itself.

All electronic equipment and systems sold in the United States must pass standards established by the Federal Communication Commission (FCC). This application note addresses the issue of electromagnetic compatibility and defines some guidelines for noise reduction techniques both at the device and the circuit board levels. Following these industry-proven guidelines can help a given system pass the FCC requirements for reducing electromagnetic interference.

### Definition of Interference

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Interference occurs when received energy causes a receptor to behave in an undesired manner. This interference occurs either directly (through a conductor, common impedance coupling, etc.) or indirectly (through crosstalk and radiation coupling) as shown in **Figure 1**. Although the focus of this application note is on radiated emission, the rules and the guidelines presented here apply to conducted emissions as well.

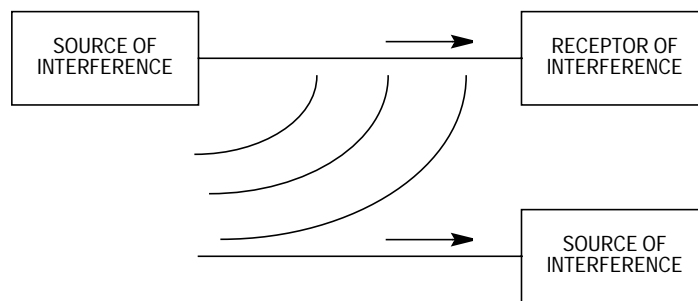


**Figure 1. Direct and Indirect Interference Paths**

## Sources of EMI

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Electromagnetic interference occurs through conduction and through radiation. Numerous sources of electromagnetic emissions such as lightning, relays, dc electric motors, and fluorescent lights can cause interference (see [Figure 2](#)). Undesirable signals may be radiated or received by ac power conductors, interconnection cables, metallic cabinets, and the internal circuitry of subsystems.



**Figure 2. Sources of Electromagnetic Emissions**

In high-speed digital circuits, the clock circuitry is usually the biggest generator of wide-band noise. In faster MCUs, these circuits can produce harmonic distortions up to 300 MHz, which should be eliminated. In digital circuits, the most vulnerable elements are the reset lines, interrupt lines, and control lines.

## Conductive EMI

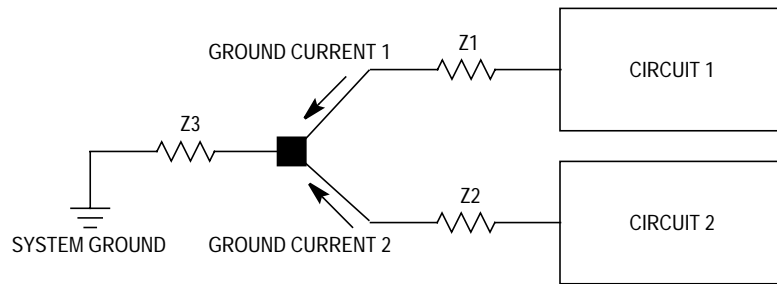
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One of the most obvious, but often overlooked, ways to induce noise into a circuit is via a conductor. A wire run through a noisy environment can pick up noise and conduct it to another circuit, where it causes interference. The designer must either prevent the wire from picking up noise or remove noise by decoupling before it causes interference. The most common example is noise conducted into a circuit on the power supply leads. If the supply itself, or other circuits connected to the

supply, are sources of interference, it becomes necessary to decouple before the power conductors enter the susceptible circuit.

## Coupling through Common Impedance

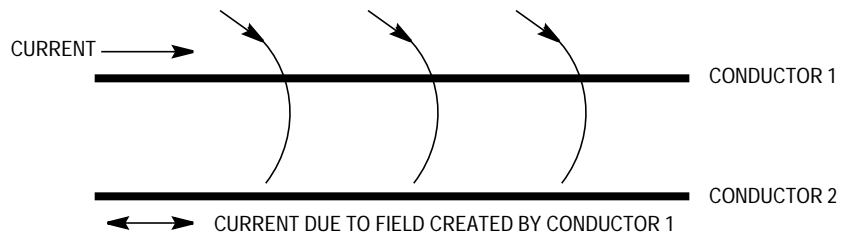
This type of coupling occurs when currents from two different circuits flow through a common impedance. The voltage drop across the impedance is influenced by both circuits. **Figure 3** shows the classic example. Ground currents from both circuits flow through the common ground impedance. The ground potential of circuit 1 is modulated by ground current 2. A noise signal or a dc offset is coupled from circuit 2 to circuit 1 through the common ground impedance.



**Figure 3. Common Impedance Coupling**

## Coupling through Radiation

Coupling through radiation, commonly called crosstalk, occurs when a current flowing through a conductor creates an electromagnetic field which induces a transient current in another nearby conductor, as shown in **Figure 4**.



**Figure 4. Radiation Coupling**

**Radiated Emission** The two basic types of radiated emission are differential mode (DM) and common mode (CM).

Common-mode radiation or monopole antenna radiation is caused by unintentional voltage drops that raise all the ground connections in a circuit above system ground potential. The electric field term for CM is:

$$E = 4 (1) 10^{-7} (f L I_f/d) \text{ volts/meter}$$

Where:

f = frequency in Hz

L = cable length in m

d = distance from cable in m

$I_f$  = CM current in cable at frequency  $f_A$

Differential-mode radiation occurs when an alternating current passes through a small loop. The magnitude of the radiation from the loop varies in proportion to the current. The electric field term for DM is:

$$E = 265 (10^{-16}) (A I_f f^2/d) \text{ volts/meter}$$

Where:

A = loop area in  $m^2$

d = distance from loop center in m

$I_f$  = current at frequency A in Hz

f = frequency (of harmonic) in Hz

For example, at a frequency of 100 MHz and a distance of 3 m, the electric fields for CM and DM are:

$$E_{CM} = 1 \text{ mV/m @ } I = 25 \text{ } \mu\text{A and } L = 1 \text{ m}$$
$$E_{DM} = 220 \text{ } \mu\text{V/m @ } I = 25 \text{ mA and } A = 1 \text{ cm}^2$$

Due to the magnitude of the electric field, CM radiation is much more of an emission problem than DM radiation. To minimize CM radiation, common current must be reduced to zero by means of a sensible grounding scheme.

## Factors that Affect EMC

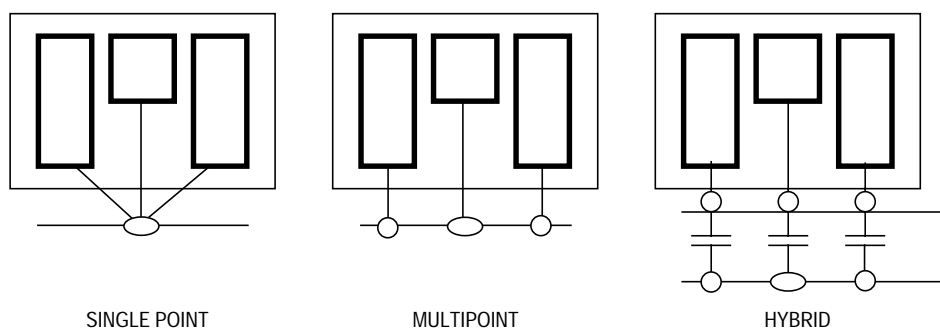
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**Voltage** Higher supply voltages mean greater voltage swings and more emissions. Lower supply voltages can affect susceptibility.

**Frequency** Higher frequency yields more emissions. Periodic signals generate more emissions. High-frequency digital systems create current spikes when transistors are switched on and off. Analog systems create current spikes when load currents change.

**Grounding** Nothing is more important to circuit design than a solid and complete power system. An overwhelming majority of all EMC problems, whether they are due to emissions, susceptibility, or self compatibility, have inadequate grounding as a principal contributor.

There are three types of signal grounding: single point, multipoint and hybrid, as shown in [Figure 5](#). The single-point ground is acceptable at frequencies below 1 MHz, but not at high frequency due to the high impedance. Multipoint grounding is best for high-frequency applications, such as digital circuitry. Hybrid grounding uses a single-point ground for low frequency and multipoint ground for high frequency.

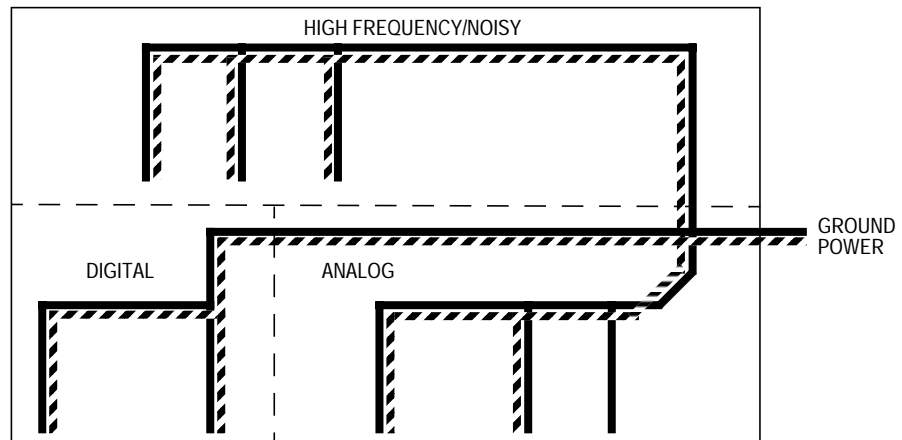


**Figure 5. Grounding Schemes**

Ground layout is especially critical (refer to [Figure 6](#)). Ground returns from high-frequency digital circuits and low-level analog circuits must not be mixed.

**Integrated Circuit Design** Die size, manufacturing technology, pad layout (multiple ground and power pins better) and packaging can all affect EMI.

**PCB Design** Proper printed circuit board (PCB) layout is essential to prevention of EMI. "Do's and don'ts" of PCB layout are outlined in [Noise Reduction Techniques](#).



**Figure 6. Preferred Ground and Power Plane Layout**

### Power Decoupling

When a logic gate switches, a transient current is produced on power supply lines. These transient currents must be damped and filtered out. High-frequency ceramic capacitors with low-inductance are ideal for this purpose. Subsequent sections discuss capacitors and filtering techniques.

Transient currents from high  $di/dt$  sources cause ground and trace "bounce" voltages. The high  $di/dt$  generates a broad range of high-frequency currents that excite structures and cables to radiate. A variation in current through a conductor with a certain inductance,  $L$ , results in a voltage drop of:

$$V = L \cdot di/dt$$

The voltage drop can be minimized by reducing either the inductance or the variation in current over time.

## Noise Reduction Techniques

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Three ways to prevent interference are:

1. Suppress the emission at its source.
2. Make the coupling path as inefficient as possible.
3. Make the receptor less susceptible to emission.

The following paragraphs describe commonly used noise reduction techniques at the device and PCB levels. Motorola uses all the device-level techniques described. The suggested PCB techniques are not an EMI complete solution, but implementing them can greatly affect the performance of a noisy system.

### Device-Level Techniques

Device-level noise-reduction techniques include:

- Use multiple power and ground pins
- Use fewer clocks
- Eliminate fights or race conditions
- Reduce output buffer drive
- Use low-power techniques
- Reduce internal power/ground trace impedance
- For long buses, keep high-speed traces separated from low-speed traces. Add extra spacing between high-speed and low-speed signals and run high-frequency signals next to a ground bus.
- Supply good ground imaging for long traces, high-speed signals
- Turn off clocks when not in use
- Eliminate charge pumps if possible
- Minimize loop area within chip

### Board-Level Techniques

Board structure, routing, and filtering board-level techniques are discussed here.

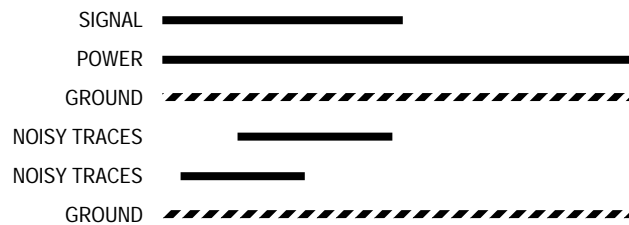
#### *Board Structure*

Board-structure noise-reduction techniques include:

- Use ground and power planes
- Maximize plane areas to provide low impedance for power supply decoupling
- Minimize surface conductors
- Use narrow traces (4 to 8 mils) to increase high-frequency damping and reduce capacitive coupling



- Segment ground/power for digital, analog, receiver, transmitter, relays, etc.
- Separate circuits on PCB according to frequency and type
- Do not notch PCB; traces routed around notches can cause unwanted loops
- Use multilayer boards to enclose traces between power and ground planes as shown in [Figure 7](#).



**Figure 7. Multilayer Board Layout**

- Avoid large open-loop plane structures
- Border PCB with chassis ground; this provides a formidable shield (or field interceptor) to prevent radiation (or reduce susceptibility) at the circuit boundaries.
- Use multipoint grounding to keep ground impedance low at high frequencies
- Use single-point grounding only for low-frequency, low-level circuits
- Keep ground leads shorter than one-twentieth ( $1/20$ ) of a wavelength to prevent radiation and to maintain low impedance

### *Routing*

Routing noise-reduction techniques include:

- Use 45-degree, rather than 90-degree, trace turns. Ninety-degree turns add capacitance and cause change in the characteristic impedance of the transmission line.
- Keep spacing between adjacent active traces greater than trace width to minimize crosstalk.
- Keep clock signal loop areas as small as possible.
- Keep high-speed lines and clock-signal conductors short and direct.

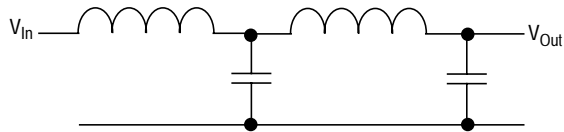
- Do not run sensitive traces parallel to traces that carry high-current, fast-switching signals.
- Eliminate floating digital inputs to prevent unnecessary switching and noise generation:
  - Configure multipurpose device pins as outputs.
  - Set three-state pins to high impedance.
  - Use appropriate pullup or pulldown circuitry.
- Avoid running traces under crystals and other inherently noisy circuits.
- Run corresponding power and ground and signal and return traces in parallel to cancel noise.
- Keep clock traces, buses, and chip-enable lines separate from input/output (I/O) lines and connectors.
- To protect critical traces:
  - Use 4-mil to 8-mil traces to minimize inductance.
  - Route close to ground plane.
  - Sandwich between planes.
  - Guardband with a ground on each side.
- Use orthogonal crossovers for traces and intersperse ground traces to minimize crosstalk, especially when analog and digital signals are routed together.
- Route clock signals perpendicular to I/O signals.

### *Filtering*

Filter techniques include:

- Filter the power line and all signals entering a board.
- Use high-frequency, low-inductance ceramic capacitors for integrated circuit (IC) decoupling at each power pin (0.1  $\mu\text{F}$  for up to 15 MHz, 0.01  $\mu\text{F}$  over 15 MHz).
- Use tantalum electrolytic capacitors as bulk decoupling capacitors at headers and connectors. Bulk decoupling capacitors recharge the IC decoupling capacitors.
- Bypass all power feed and reference voltage pins for analog circuits.
- Bypass fast switching transistors.

- Decouple locally whenever possible.
- Decouple power/ground at device leads.
- Use ferrite beads at power entry points. Beads are an inexpensive and convenient way to attenuate frequencies above 1 MHz without causing power loss at low frequencies. They are small and can generally be slipped over component leads or conductors.
- Use multistage filtering to attenuate multiband power supply noise as shown in **Figure 8**.



**Figure 8. Multistaging Filtering**

## Other Design Techniques

Other design techniques include:

- Mount crystals flush to board and ground them.
- Use shielding where appropriate.
- Use the lowest frequency and slowest rise time clock that will do the job.
- Use series termination to minimize resonance and transmission reflection. Impedance mismatch between load and line causes a portion of the signal to reflect. Reflections induce ringing and overshoot, producing significant EMI. Termination is needed when line length,  $L$ , (inches) exceeds  $3 t_r$  (ns). The value of the termination resistor is given by:

$$R_L = Z_0 / (1 + C_L / C_{Line})^{1/2} \quad (2)$$

Where:

$Z$  = Characteristic impedance of the line without the load(s)

$C_L$  = Total load distributed along the line

$C_{Line}$  = Total capacitance of the line without the load(s)

- Route adjacent ground traces closer to signal traces than other signal traces for more effective interception of emerging fields.

- Place properly decoupled line drivers and receivers as close as practical to the physical I/O interface. This reduces coupling to other PCB circuitry and lowers both radiation and susceptibility.
- Shield and twist noisy leads together to cancel mutual coupling out of the PCB.
- Use clamping diodes for relay coils and other inductive loads.

## References


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