Using D-Bug12 With the MC9S12DP256 0K79X Mask Set or the MC9S12H256 0K78X Mask Set

An errata was introduced in the BDM module on the MC9S12DP256 (Barracuda II) 0K79X mask set and the MC9S12H256 (Mako) 0K78X mask set. When using EXTAL ÷ 2 as the BDM clock source (default) and the PLL is selected as the bus clock source, BDM communications will be lost when the PLL multiplier is greater than 2 ((synr+1))/(refdv+1)). Once communication is lost, the only way to regain communications is to reset the target MCU.

D-Bug12 version 4.0.0b8 and later has been modified to configure the BDM to use the target bus clock (BDM Status Register CLKSW=1) if either of these parts is connected as the target device. Because the BDM interface is being driven by the target bus clock, BDM communication will be lost if the target firmware changes the bus clock frequency using the PLL. To prevent the loss of communications from disrupting a debug session, a command has been added to D-Bug12 that allows an alternate BDM communication clock frequency to be specified. If BDM communication with the target is lost, D-Bug12 will automatically attempt communication at the alternate frequency without notifying the user.

The ALTCLK command (see documentation) is used to specify the alternate BDM communication frequency, which should be equal to the target bus frequency with the PLL engaged as the bus clock. For example, if a 4 MHz crystal/oscillator is being used in a target application and the firmware programs the PLL to generate a 24 MHz bus clock, the ALTCLK command should be used to specify an alternate bus frequency of 24000 KHz. The ALTCLK command must be used to specify the alternate BDM communication frequency **before** executing the target code that engages the PLL as the bus clock. Note that the alternate BDM communication rate specified using the ALTCLK command is saved in D-Bug12's host MCU EEPROM so that it does not have to be reentered each time the development tool is powered up.

Note: Switching between the two BDM communications rates is completely transparent to the developer with one exception. If D-Bug12's memory modify command (MM) is used to engage the PLL as the bus clock by setting the PLLSEL bit in the CLKSEL register, D-Bug12 will report that the target memory could not be modified, because of the temporary loss of communications. However, after displaying the error message, D-Bug12 will resynchronize to the new BDM communications rate and show that the target memory was properly modified.
