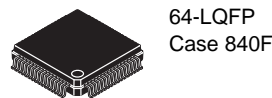




## MC9S08LL16 Series

### Covers: MC9S08LL16 and MC9S08LL8



64-LQFP  
Case 840F



48-LQFP  
Case 932



48-QFN  
1314

#### Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20-MHz CPU at 3.6V to 1.8V across temperature range of -40°C to 85°C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Dual Array FLASH read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and FLASH contents
- Power-Saving Modes
  - Two low power stop modes
  - Reduced power wait mode
  - Low power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents.
  - Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
  - 6  $\mu$ s typical wake up time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1MHz to 10 MHz.
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-Voltage Warning with interrupt
  - Low-Voltage Detection with reset or interrupt
  - Illegal Opcode Detection with reset
  - Illegal address Detection with reset
  - FLASH block protection
- Development Support
  - Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — 4x28 or 8x24 LCD driver with internal charge pump and option to provide an internally regulated LCD reference that can be trimmed for contrast control.
  - **ADC** — 8-channel, 12-bit resolution; 2.5  $\mu$ s conversion time; automatic compare function; temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
  - **ACMP** — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
  - **SPI** — Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
  - **IIC** — IIC with up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
  - **TPMx** — Two 2-channel (TPM1 and TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel;
  - **TOD** — (Time Of Day) 8-bit quarter second counter with match register; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components.
- Input/Output
  - 38 GPIOs, 2 output-only pins
  - 8 KBI interrupts with selectable polarity
  - Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins.
- Package Options
  - 64-LQFP, 48-LQFP, 48-QFN

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**Preliminary**  
**Subject to Change Without Notice**

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## Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	9/2008	Initial Release.
2	10/2008	Updated electrical characteristics.

## Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>

### Reference Manual (MC9S08LL16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

# 1 Devices in the MC9S08LL16 Series

Table 1 summarizes the feature set available in the MC9S08LL16 Series series of MCUs.

**Table 1. MC9S08LL16 Series Features by MCU and Package**

Feature	MC9S08LL16		MC9S08LL8
	64-pin LQFP	48-pin QFN/LQFP	48-pin QFN/LQFP
FLASH	16,384 (Dual 8K Arrays)		10,240 (8K and 2K arrays)
RAM	2080	2080	2080
ACMP	yes	yes	yes
ADC	8-ch	8-ch	8-ch
IIC	yes	yes	yes
IRQ	yes	yes	yes
KBI	8	8	8
SCI	yes	yes	yes
SPI	yes	yes	yes
TPM1	2-ch	2-ch	2-ch
TPM2	2-ch	-	-
TOD	Yes	Yes	Yes
LCD	8x24 4x28	8x16 4x20	8x16 4x20
I/O pins <sup>1</sup>	38	31	31

<sup>1</sup>I/O does not include two output-only port pins.

The block diagram in [Figure 1](#) shows the structure of the MC9S08LL16 Series MCU.

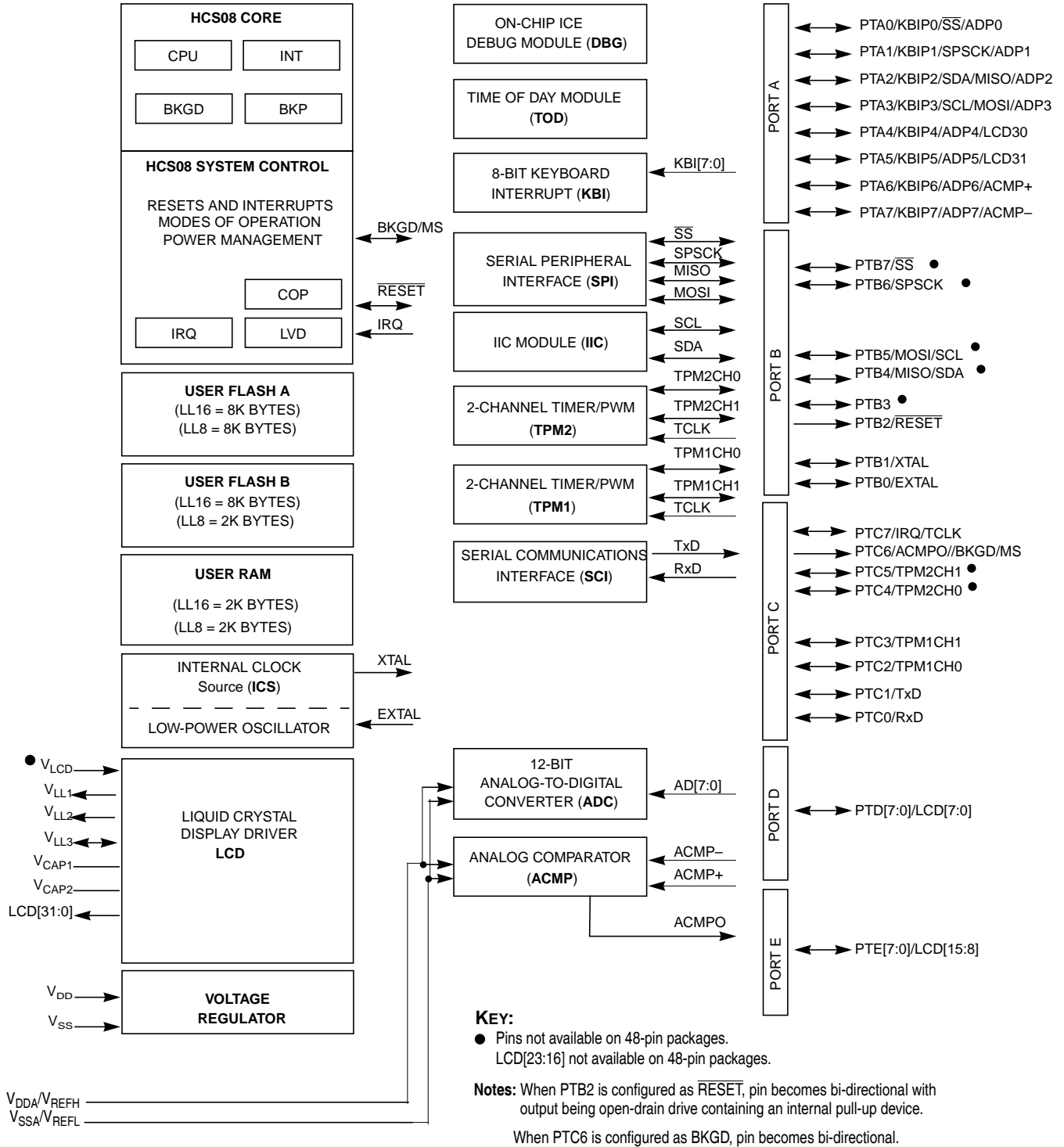
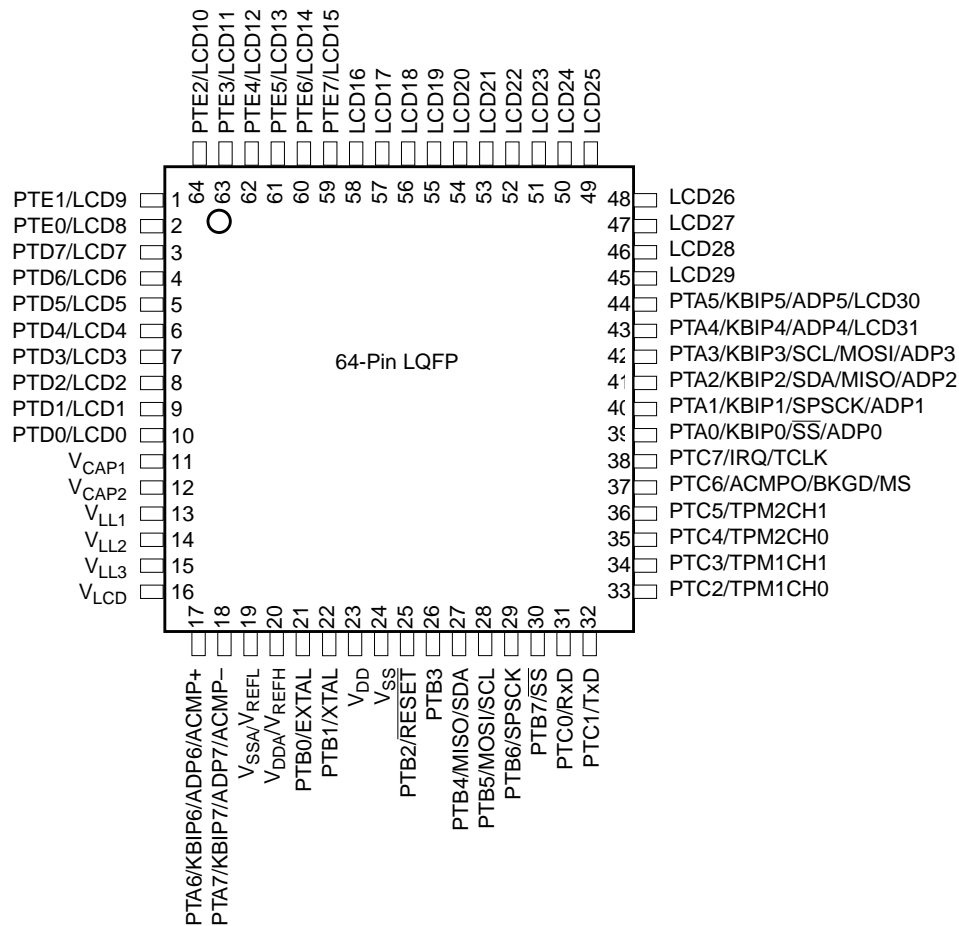


Figure 1. MC9S08LL16 Series Block Diagram

## 2 Pin Assignments

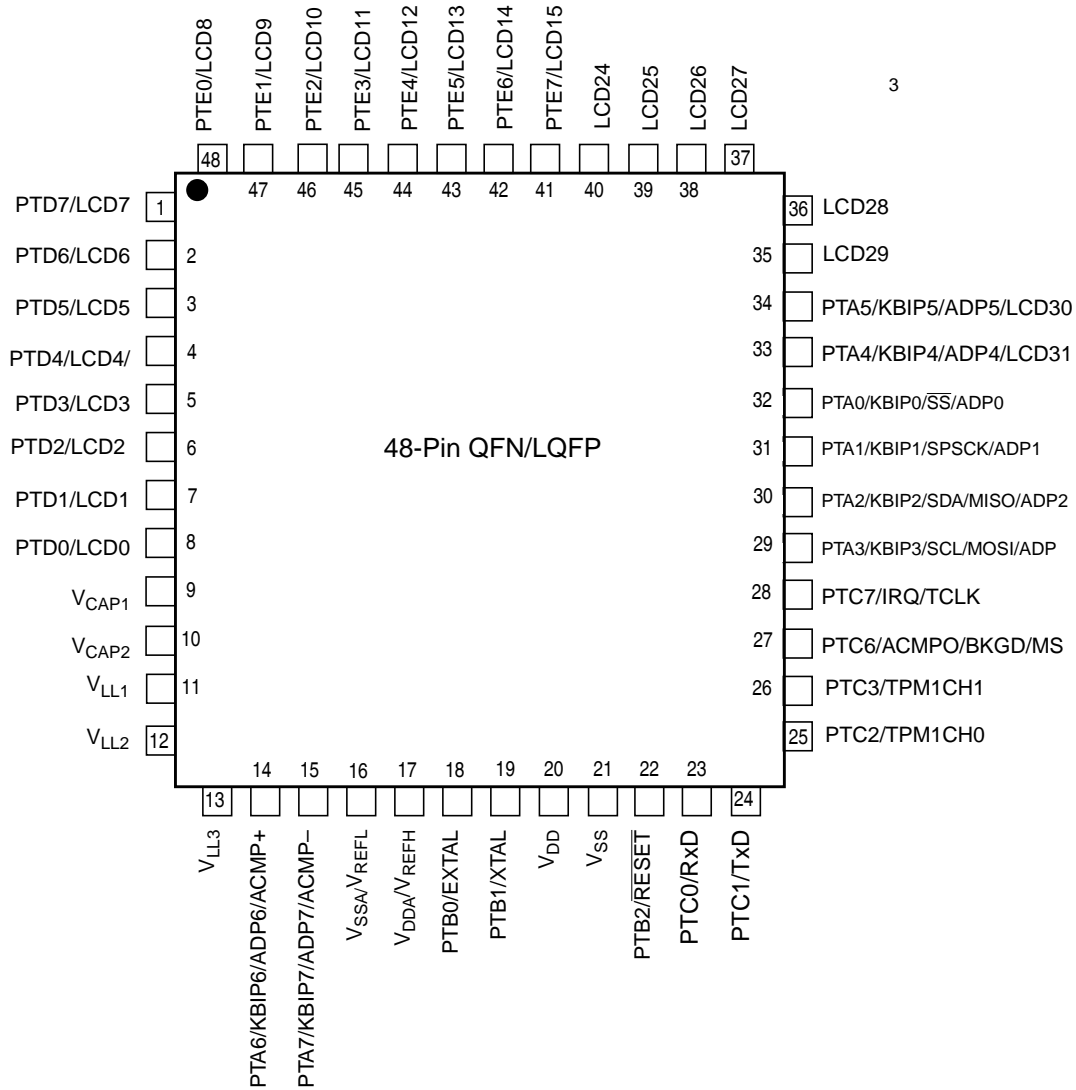
This section shows the pin assignments for the MC9S08LL16 Series devices.



Note:  $V_{REFH}/V_{REFL}$  are internally connected to  $V_{DDA}/V_{SSA}$ .

Figure 2. 64-pin LQFP

## Pin Assignments



Note: V<sub>REFH</sub>/V<sub>REFL</sub> are internally connected to V<sub>DDA</sub>/V<sub>SSA</sub>

Figure 3. 48-pin QFN/LQFP

Table 2. Pin Availability by Package Pin-Count

		<-- Lowest Priority --> Highest				
64	48	Port Pin	Alt 1	Alt 2	Alt3	Alt4
1	47	PTE1	LCD9			
2	48	PTE0	LCD8			
3	1	PTD7	LCD7			
4	2	PTD6	LCD6			
5	3	PTD5	LCD5			
6	4	PTD4	LCD4			
7	5	PTD3	LCD3			
8	6	PTD2	LCD2			
9	7	PTD1	LCD1			
10	8	PTD0	LCD0			
11	9		V <sub>cap1</sub>			
12	10		V <sub>cap2</sub>			
13	11		V <sub>LL1</sub>			
14	12		V <sub>LL2</sub>			
15	13		V <sub>LL3</sub>			
16	—		V <sub>LCD</sub>			
17	14	PTA6	KBIP6	ADP6	ACMP+	
18	15	PTA7	KBIP7	ADP7	ACMP-	
19	16				V <sub>SSA</sub>	
					V <sub>REFL</sub>	
20	17				V <sub>REFH</sub>	
					V <sub>DDA</sub>	
21	18	PTB0		EXTAL		
22	19	PTB1		XTAL		
23	20				V <sub>DD</sub>	
24	21				V <sub>SS</sub>	
25	22	PTB2	RESET			
26	—	PTB3				
27	—	PTB4	—	MISO	SDA	
28	—	PTB5	—	MOSI	SCL	
29	—	PTB6	—	SPSCK		
30	—	PTB7	—	$\overline{SS}$		
31	23	PTC0		RxD		
32	24	PTC1		TxD		
33	25	PTC2		TPM1CH0		
34	26	PTC3		TPM1CH1		
35	—	PTC4		TPM2CH0		
36	—	PTC5		TPM2CH1		
37	27	PTC6	ACMPO	BKGD	MS	
38	28	PTC7		IRQ	TCLK	

**Table 2. Pin Availability by Package Pin-Count**

		<-- Lowest <b>Priority</b> --> Highest				
<b>64</b>	<b>48</b>	<b>Port Pin</b>	<b>Alt 1</b>	<b>Alt 2</b>	<b>Alt3</b>	<b>Alt4</b>
39	29	PTA0	KBIP0	—	SS	ADP0
40	30	PTA1	KBIP1	—	SPSCK	ADP1
41	31	PTA2	KBIP2	SDA	MISO	ADP2
42	32	PTA3	KBIP3	SCL	MOSI	ADP3
43	33	PTA4	KBIP4	ADP4	LCD31	
44	34	PTA5	KBIP5	ADP5	LCD30	
45	35		LCD29			
46	36		LCD28			
47	37		LCD27			
48	38		LCD26			
49	39		LCD25			
50	40		LCD24			
51	—		LCD23			
52	—		LCD22			
53	—		LCD21			
54	—		LCD20			
55			LCD19			
56			LCD18			
57			LCD17			
58			LCD16			
59	41	PTE7	LCD15			
60	42	PTE6	LCD14			
61	43	PTE5	LCD13			
62	44	PTE4	LCD12			
63	45	PTE3	LCD11			
64	46	PTE2	LCD10			

### 3 Electrical Characteristics

#### 3.1 Introduction

This section contains electrical and timing specifications for the MC9S08LL16 Series of microcontrollers available at the time of publication.

#### 3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:



**Table 3. Parameter Classifications**

<b>P</b>	Those parameters are guaranteed during production testing on each individual device.
<b>C</b>	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
<b>T</b>	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
<b>D</b>	Those parameters are derived mainly from simulations.

**NOTE**

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

**3.3 Absolute Maximum Ratings**

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

**Table 4. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to +3.8	V
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Digital input voltage	$V_{In}$	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	$\pm 25$	mA
Storage temperature range	$T_{stg}$	-55 to 150	°C

<sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.

<sup>2</sup> All functional non-supply pins, except for PTB2 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

### 3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 5. Thermal Characteristics**

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	$T_A$	$T_L$ to $T_H$ -40 to 85	°C
Maximum junction temperature	$T_J$	95	°C
Thermal resistance Single-layer board			
64-pin LQFP	$\theta_{JA}$	72	°C/W
48-pin QFN		84	
48-pin LQFP		81	
Thermal resistance Four-layer board			
64-pin LQFP	$\theta_{JA}$	54	°C/W
48-pin QFN		30	
48-pin LQFP		57	

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 3-1}$$

where:

$T_A$  = Ambient temperature, °C

$\theta_{JA}$  = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$ , Watts — chip internal power

$P_{I/O}$  = Power dissipation on input and output pins — user determined

For most applications,  $P_{I/O} \ll P_{int}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 3-2}$$

Solving Equation 3-1 and Equation 3-2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3-3}$$

where  $K$  is a constant pertaining to the particular part.  $K$  can be determined from equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of  $K$ , the values of  $P_D$  and  $T_J$  can be obtained by solving Equation 3-1 and Equation 3-2 iteratively for any value of  $T_A$ .

### 3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

**Table 6. ESD and Latch-up Test Conditions**

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	$\Omega$
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Charge Device Model	Series resistance	R1	0	$\Omega$
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

**Table 7. ESD and Latch-Up Protection Characteristics**

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{HBM}$	$\pm 2000$	—	V
2	Charge device model (CDM)	$V_{CDM}$	$\pm 500$	—	V
3	Latch-up current at $T_A = 85^\circ\text{C}$	$I_{LAT}$	$\pm 100$	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

### 3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

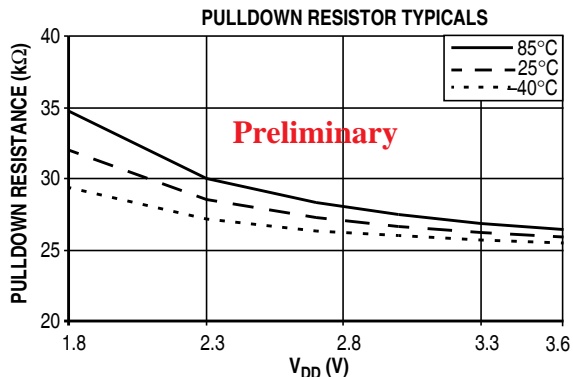
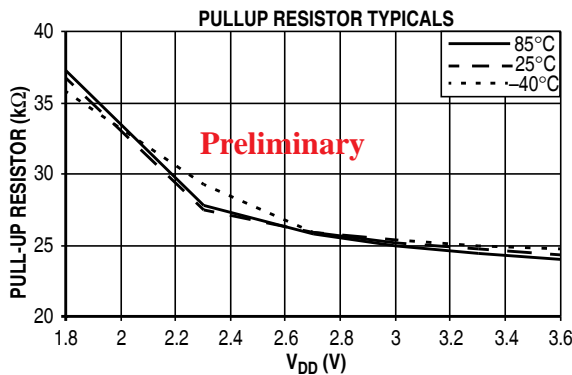
**Table 8. DC Characteristics**

Num	C	Characteristic	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
1		Operating Voltage			1.8		3.6	V
2	C	Output high voltage PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7] <sup>2</sup> , low-drive strength	V <sub>OH</sub>	1.8 V, I <sub>Load</sub> = -2 mA	V <sub>DD</sub> - 0.5	—	—	V
	P	PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7] <sup>2</sup> , high-drive strength		2.7 V, I <sub>Load</sub> = -10 mA	V <sub>DD</sub> - 0.5	—	—	
	C	PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7] <sup>2</sup> , high-drive strength		1.8 V, I <sub>Load</sub> = -3 mA	V <sub>DD</sub> - 0.5	—	—	
3	C	Output high voltage PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V <sub>OH</sub>	1.8 V, I <sub>Load</sub> = -1 mA	V <sub>DD</sub> - 0.8	—	—	V
	P	PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		2.7 V, I <sub>Load</sub> = -5 mA	V <sub>DD</sub> - 0.8	—	—	
	C	PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		1.8 V, I <sub>Load</sub> = -1 mA	V <sub>DD</sub> - 0.5	—	—	
4	D	Output high current Max total I <sub>OH</sub> for all ports	I <sub>OHT</sub>		—	—	100	mA
5	C	Output low voltage PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], low-drive strength	V <sub>OL</sub>	1.8 V, I <sub>Load</sub> = 2 mA	—	—	0.5	V
	P	PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		2.7 V, I <sub>Load</sub> = 10 mA	—	—	0.5	
	C	PTA[0:3], PTA[6:7], PTB[0:7], PTC[0:7], high-drive strength		1.8 V, I <sub>Load</sub> = 3 mA	—	—	0.5	
6	C	Output low voltage PTA[4:5], PTD[0:7], PTE[0:7], low-drive strength	V <sub>OL</sub>	1.8 V, I <sub>Load</sub> = 1 mA	—	—	0.8	V
	P	PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		2.7 V, I <sub>Load</sub> = 5 mA	—	—	0.8	
	C	PTA[4:5], PTD[0:7], PTE[0:7], high-drive strength		1.8 V, I <sub>Load</sub> = 1 mA	—	—	0.5	
7	D	Output low current Max total I <sub>OL</sub> for all ports	I <sub>OLT</sub>		—	—	100	mA
8	P	Input high voltage all digital inputs	V <sub>IH</sub>	V <sub>DD</sub> > 2.7 V	0.70 x V <sub>DD</sub>	—	—	V
	C	all digital inputs		V <sub>DD</sub> > 1.8 V	0.85 x V <sub>DD</sub>	—	—	
9	P	Input low voltage all digital inputs	V <sub>IL</sub>	V <sub>DD</sub> > 2.7 V	—	—	0.35 x V <sub>DD</sub>	
	C	all digital inputs		V <sub>DD</sub> > 1.8 V	—	—	0.30 x V <sub>DD</sub>	
10	C	Input hysteresis all digital inputs	V <sub>hys</sub>		0.06 x V <sub>DD</sub>	—	—	mV
11	P	Input leakage current all input only pins (Per pin)	I <sub>In</sub>	V <sub>In</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	0.1	1	μA
12	P	Hi-Z (off-state) leakage current all input/output (per pin)	I <sub>OZ</sub>	V <sub>In</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	0.1	1	μA

**Table 8. DC Characteristics (continued)**

Num	C	Characteristic	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
13	P	Pullup, all digital inputs, when enabled Pull-down resistors	$R_{PU}$ , $R_{PD}$		17.5	—	52.5	k $\Omega$
14	D	DC injection current <sup>3, 4, 5</sup> Single pin limit Total MCU limit, includes sum of all stressed pins	$I_{IC}$	$V_{IN} < V_{SS}$ , $V_{IN} > V_{DD}$	-0.2	—	0.2	mA
					-5	—	5	mA
15	C	Input Capacitance, all pins	$C_{In}$		—	—	8	pF
16	C	RAM retention voltage	$V_{RAM}$		—	0.6	1.0	V
17	C	POR re-arm voltage <sup>6</sup>	$V_{POR}$		0.9	1.4	2.0	V
18	D	POR re-arm time	$t_{POR}$		10	—	—	$\mu$ s
19	P	Low-voltage detection threshold	$V_{LVD}$	$V_{DD}$ falling $V_{DD}$ rising	1.80	1.84	1.88	V
					1.88	1.92	1.96	V
20	P	Low-voltage warning threshold	$V_{LVW}$	$V_{DD}$ falling $V_{DD}$ rising	2.08	2.14	2.2	V
21	P	Low-voltage inhibit reset/recover hysteresis	$V_{hys}$		—	80	—	mV
22	P	Bandgap Voltage Reference <sup>7</sup>	$V_{BG}$		1.16	1.17	1.18	V

- <sup>1</sup> Typical values are measured at 25°C. Characterized, not tested
- <sup>2</sup> All I/O pins except for LCD pins in Open Drain mode.
- <sup>3</sup> All functional non-supply pins, except for PTB2 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .
- <sup>4</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
- <sup>5</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If the positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure that external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).
- <sup>6</sup> POR will occur below the minimum voltage.
- <sup>7</sup> Factory trimmed at  $V_{DD} = 3.0$  V, Temp = 25°C



**Table 9. All I/O Pullup and Pulldown Typical Resistor Values ( $V_{DD} = 3.0$  V)**

Electrical Characteristics

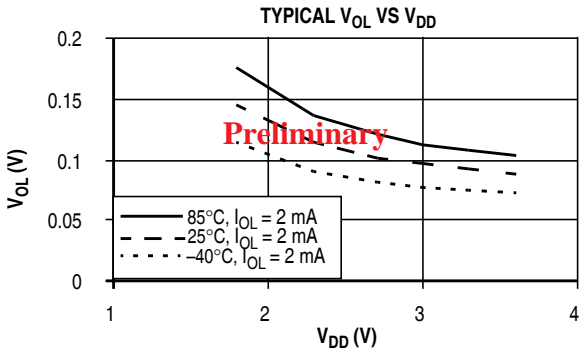
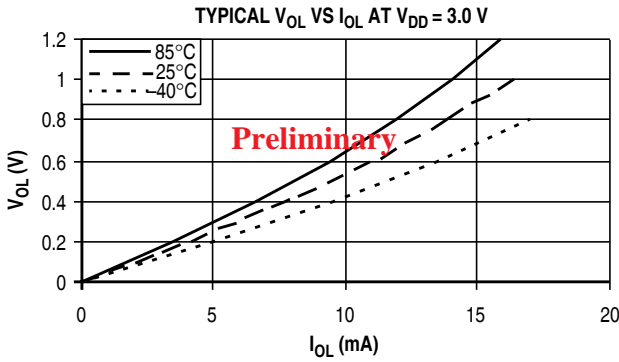


Table 10. Typical Low-Side Driver (Sink) Characteristics (Non LCD pins)— Low Drive (PTxDSn = 0)

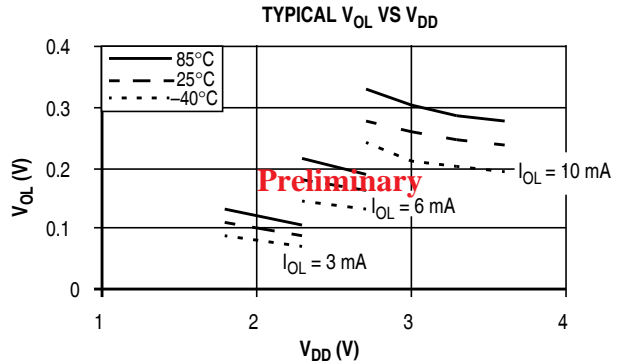
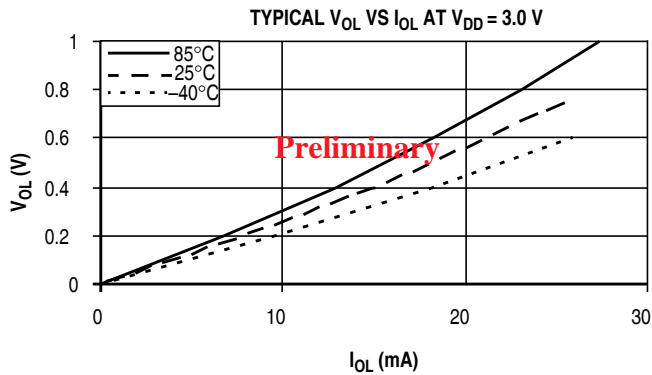


Table 11. Typical Low-Side Driver (Sink) Characteristics (Non LCD pins) — High Drive (PTxDSn = 1)

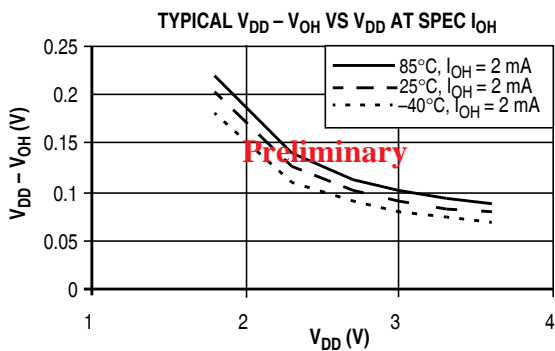
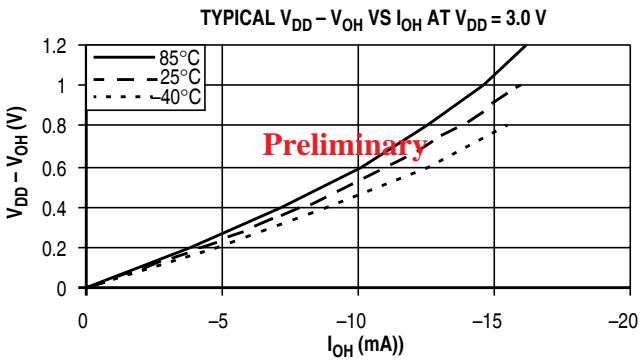


Table 12. Typical High-Side (Source) Characteristics (Non LCD pins)— Low Drive (PTxDSn = 0)

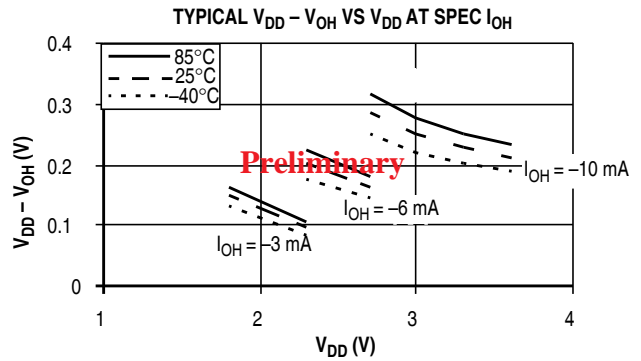
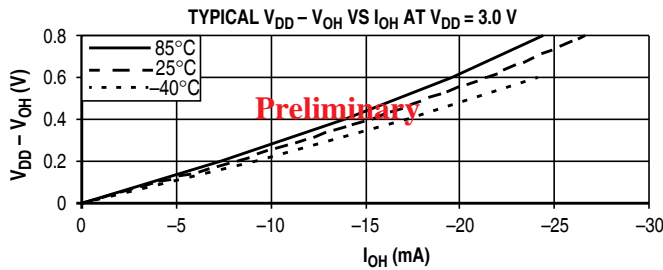


Table 13. Typical High-Side (Source) Characteristics(Non LCD pins) — High Drive (PTxDSn = 1)

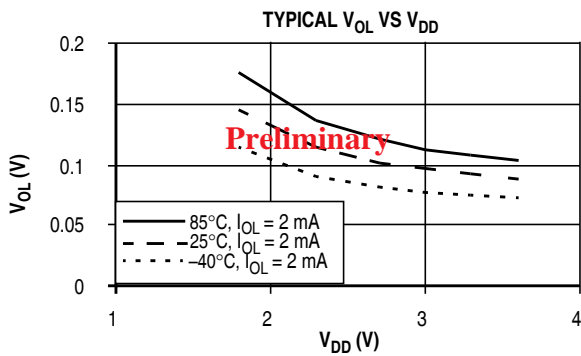
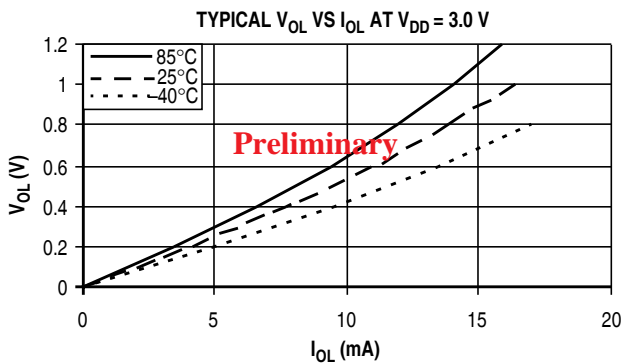


Table 14. Typical Low-Side Driver (Sink) Characteristics (LCD/GPIO pins) — Low Drive (PTxDSn = 0)

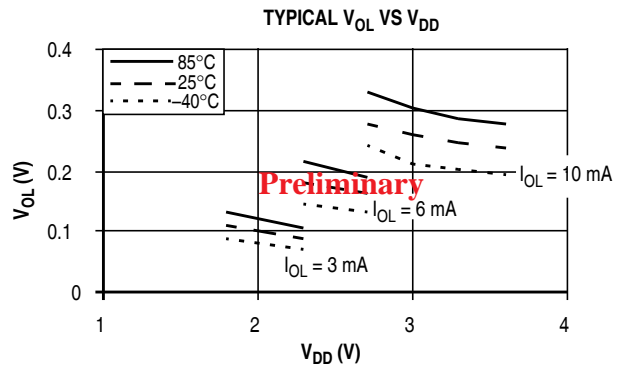
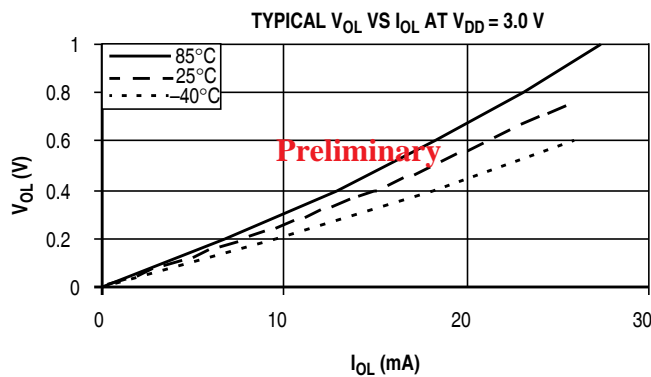


Table 15. Typical Low-Side Driver (Sink) Characteristics(LCD/GPIO pins) — High Drive (PTxDSn = 1)

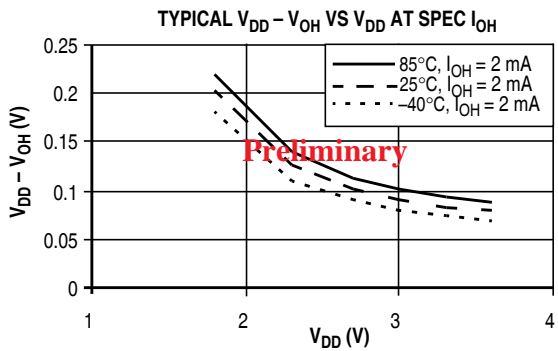
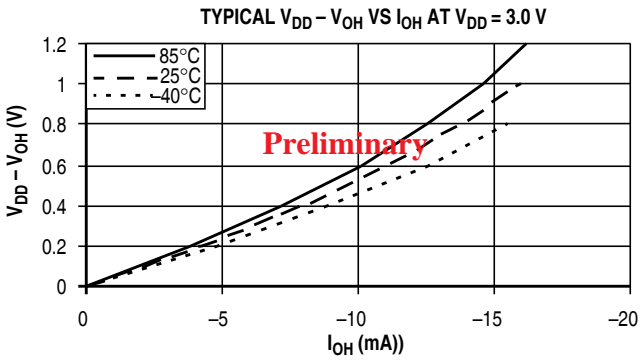


Table 16. Typical High-Side (Source) Characteristics (LCD/GPIO pins)— Low Drive (PTxDSn = 0)

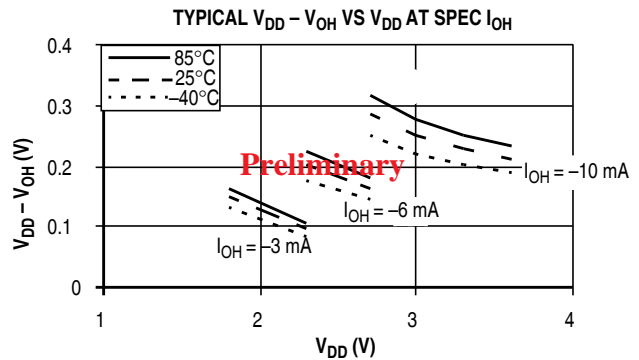
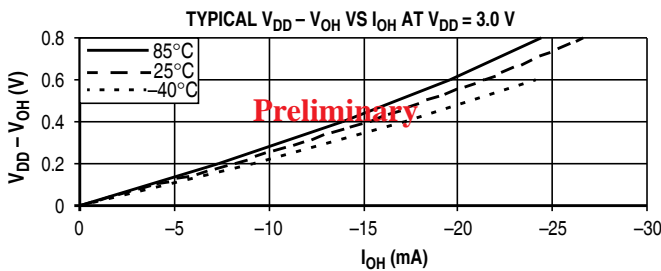


Table 17. Typical High-Side (Source) Characteristics (LCD/GPIO pins) — High Drive (PTxDSn = 1)

### 3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 18. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V <sub>DD</sub> (V)	Typ <sup>1</sup>	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	R <sub>IDD</sub>	8 MHz	3	5.60	5.70	mA	-40 to 85°C
	1 MHz			1		1.52			
2	T	Run supply current FEI mode, all modules off	R <sub>IDD</sub>	10 MHz	3	3.60	—	mA	-40 to 85°C
	T			1 MHz		0.50	—		
3	T	Run supply current LPRS=0, all modules off	R <sub>IDD</sub>	16 kHz FBILP	3	165	—	μA	-40 to 85°C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS=1, all modules off; running from Flash	R <sub>IDD</sub>	16 kHz FBILP	3	77	—	μA	-40 to 85°C
	T			16 kHz FBELP		21	—		



Table 18. Supply Current Characteristics

Num	C	Parameter		Symbol	Bus Freq	V <sub>DD</sub> (V)	Typ <sup>1</sup>	Max	Unit	Temp (°C)	
5	T	Run supply current LPRS=1, all modules off; running from RAM		RI <sub>DD</sub>	16 kHz FBILP	3	77	—	μA	-40 to 85°C	
	T				16 kHz FBELP		7.3	—			
6	P	Wait mode supply current FEI mode, all modules off		WI <sub>DD</sub>	8 MHz	3	2.3	3.5	mA	-40 to 85°C	
	C				1 MHz		0.8	1.15			
7		Wait mode supply current LPRS = 1, all modules off		WI <sub>DD</sub>	16 kHz FBELP	3	1.3	—	μA	-40 to 85°C	
8	P	Stop2 mode supply current		S2I <sub>DD</sub>	n/a	3	300	8500	nA	-40 to 85°C	
	C				n/a	2	250	7700			
9	P	Stop3 mode supply current No clocks active		S3I <sub>DD</sub>	n/a	3	400	12300	nA	-40 to 85°C	
	C				n/a	2	350	11500			
10	C	Application Stop3 mode supply current <sup>2</sup>		ApS31 <sub>DD</sub>	n/a	3	6.1	—	μA	25°C	
11	C	Application Stop3 mode supply current <sup>2</sup>		ApS31 <sub>DD</sub>	n/a	3	7.5	—	μA	50°C	
12	T	Stop2 and Stop 3 adders:			TOD with low power crystal oscillator (LPO)	n/a	3	100	—	nA	-40 to 85°C
13					TOD with LPO	n/a	3	350	—	nA	
14					LCD <sup>3</sup> VIREG enabled Adder	n/a	3	1	20	μA	
15	T	Stop3 adders:			EREFSTEN=1	n/a	3	300	—	nA	-40 to 85°C
16					IREFSTEN=1	n/a		70	—	μA	
17					LVD	n/a		100	—	μA	
18					ACMP	n/a		20	—	μA	

<sup>1</sup> Typical values are measured at 25°C. Characterized, not tested.

<sup>2</sup> 32 kHz crystal enabled in low power mode. TOD module enabled. V<sub>I</sub>REG enabled for 3 V LCD glass 500pf 8x24 LCD glass at 32 Hz frame rate with LCD Charge pump clock set to low setting and every other segment "on."

<sup>3</sup> Adder for enabling the internally regulated voltage with no LCD glass.



Figure 4. Typical Run  $I_{DD}$  for FBE and FEI,  $I_{DD}$  vs.  $V_{DD}$   
(ACMP and ADC off, All Other Modules Enabled)

### 3.8 External Oscillator (XOSCVLP) Characteristics

Reference [Figure 5](#) and [Figure 6](#) for crystal or resonator circuits.

**Table 19. XOSCVLP and ICS Specifications (Temperature Range = -40 to 85°C Ambient)**

Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	$f_{lo}$ $f_{hi}$ $f_{hi}$	32	—	38.4	kHz MHz MHz
		Low range (RANGE = 0)		1	—	16	
		High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)		1	—	8	
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	$C_1, C_2$	See Note <sup>2</sup> See Note <sup>3</sup>			
3	D	Feedback resistor	$R_F$	—	—	—	MΩ
		Low range, low power (RANGE=0, HGO=0) <sup>2</sup>		—	10	—	
		Low range, high gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)		—	1	—	
4	D	Series resistor —	$R_S$	—	—	—	kΩ
		Low range, low power (RANGE = 0, HGO = 0) <sup>2</sup>		—	100	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	0	—	
		High range, low power (RANGE = 1, HGO = 0)		—	0	0	
		High range, high gain (RANGE = 1, HGO = 1)		—	0	10	
≥ 8 MHz	—	0	0				
4 MHz	—	0	10				
1 MHz	—	0	20				
5	C	Crystal start-up time <sup>4</sup>	$t_{CSTL}$ $t_{CSTH}$	—	600	—	ms
		Low range, low power		—	400	—	
		Low range, high gain		—	5	—	
		High range, low power High range, high gain		—	15	—	
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)	$f_{extal}$	0.03125	—	20	MHz MHz
		FEE mode		0	—	20	
		FBE or FBELP mode					

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

<sup>2</sup> Load capacitors ( $C_1, C_2$ ), feedback resistor ( $R_F$ ) and series resistor ( $R_S$ ) are incorporated internally when RANGE=HGO=0.

<sup>3</sup> See crystal or resonator manufacturer's recommendation.

<sup>4</sup> Proper PC board layout procedures must be followed to achieve specifications.

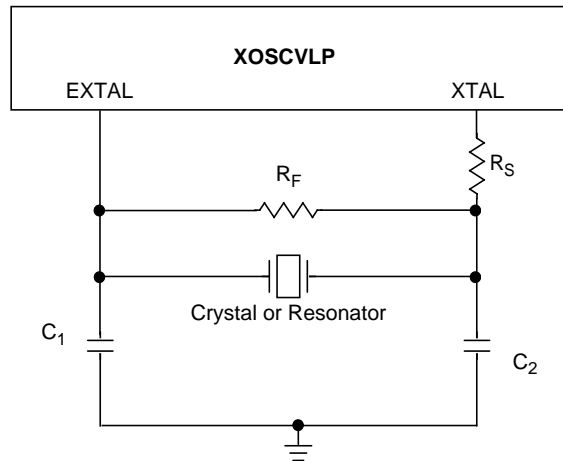


Figure 5. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

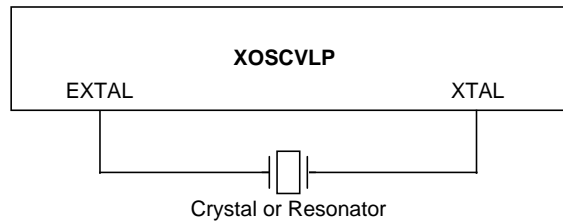


Figure 6. Typical Crystal or Resonator Circuit: Low Range/Low Power

### 3.9 Internal Clock Source (ICS) Characteristics

Table 20. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 3.6 V and temperature = 25 °C	$f_{int\_ft}$	—	32.768	—	kHz
2	P	Average internal reference frequency - trimmed	$f_{int\_t}$	31.25	—	39.063	kHz
3	T	Internal reference start-up time	$t_{IRST}$	—	—	6	μs
4	P	DCO output frequency range - untrimmed	$f_{dco\_ut}$	12.8	16.8	21.33	MHz
5	P	DCO output frequency range - trimmed	$f_{dco\_t}$	16	—	20	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	% $f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	% $f_{dco}$
8	C	Total deviation from trimmed DCO output frequency over voltage and temperature	$\Delta f_{dco\_t}$	—	+ 0.5 -1.0	± 2	% $f_{dco}$

Table 20. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
9	C	Total deviation from trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	$\Delta f_{dco\_t}$	—	± 0.5	± 1	% $f_{dco}$
10	C	FLL acquisition time <sup>2</sup>	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) <sup>3</sup>	$C_{Jitter}$	—	0.02	0.2	% $f_{dco}$

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

<sup>2</sup> This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

<sup>3</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{Bus}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via  $V_{DD}$  and  $V_{SS}$  and variation in the crystal oscillator frequency increase the  $C_{Jitter}$  percentage for a given interval.



**TBD**

Figure 7. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)



Figure 8. Deviation of DCO Output from Trimmed Frequency (20 MHz, 25°C)

## 3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

### 3.10.1 Control Timing

Table 21. Control Timing

Num	C	Rating	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	D	Bus frequency ( $t_{cyc} = 1/f_{Bus}$ )	$f_{Bus}$	dc	—	10	MHz
2	D	Internal low power oscillator period	$t_{LPO}$	700	—	1300	$\mu$ s
3	D	External reset pulse width <sup>2</sup>	$t_{extrst}$	100	—	—	ns
4	D	Reset low drive	$t_{rstdrv}$	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	$t_{MSSU}$	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes <sup>3</sup>	$t_{MSH}$	100	—	—	$\mu$ s
7	D	IRQ pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>4</sup>	$t_{ILIH}, t_{IHIL}$	100 $1.5 \times t_{cyc}$	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>4</sup>	$t_{ILIH}, t_{IHIL}$	100 $1.5 \times t_{cyc}$	— —	— —	ns
9	C	Port rise and fall time — Non-LCD Pins Low output drive (PTxDS = 0) (load = 50 pF) <sup>5, 6</sup> Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{Rise}, t_{Fall}$	— —	16 23	— —	ns
		Port rise and fall time — Non-LCD Pins High output drive (PTxDS = 1) (load = 50 pF) <sup>5, 6</sup> Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{Rise}, t_{Fall}$	— —	5 9	— —	ns

<sup>1</sup> Typical values are based on characterization data at  $V_{DD} = 3.0V$ , 25°C unless otherwise stated.

<sup>2</sup> This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

<sup>3</sup> To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of  $t_{MSH}$  after  $V_{DD}$  rises above  $V_{LVD}$ .

<sup>4</sup> This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

<sup>5</sup> Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range –40°C to 85°C.

<sup>6</sup> Except for LCD pins in Open Drain mode.

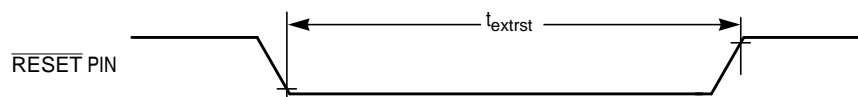


Figure 9. Reset Timing

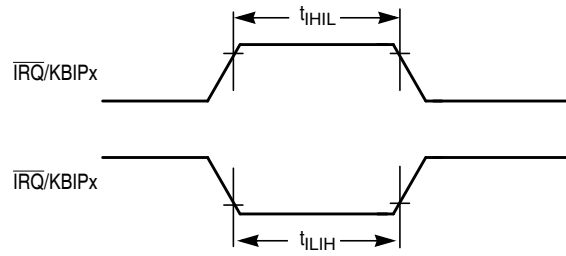


Figure 10.  $\overline{\text{IRQ}}/\text{KBIPx}$  Timing

### 3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 22. TP Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	$f_{\text{TCLK}}$	0	$f_{\text{Bus}}/4$	Hz
2	D	External clock period	$t_{\text{TCLK}}$	4	—	$t_{\text{cyc}}$
3	D	External clock high time	$t_{\text{clkh}}$	1.5	—	$t_{\text{cyc}}$
4	D	External clock low time	$t_{\text{clkl}}$	1.5	—	$t_{\text{cyc}}$
5	D	Input capture pulse width	$t_{\text{ICPW}}$	1.5	—	$t_{\text{cyc}}$

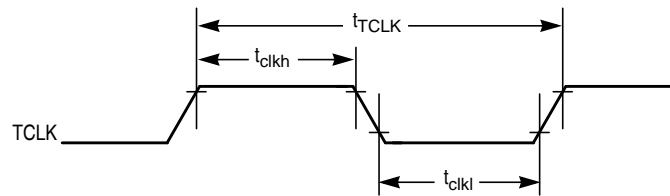


Figure 11. Timer External Clock

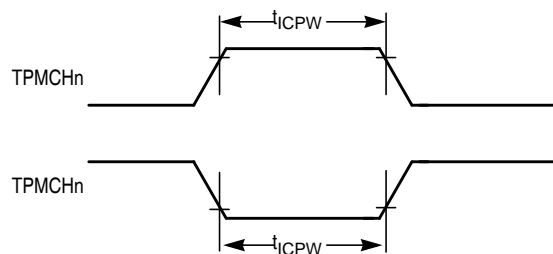


Figure 12. Timer Input Capture Pulse



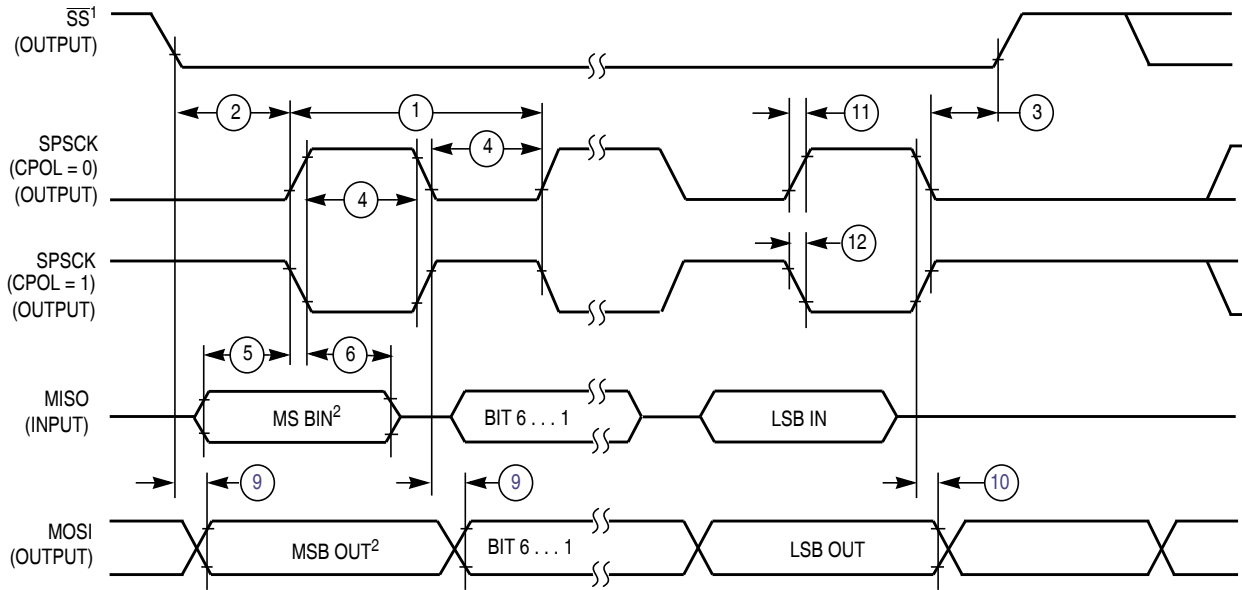
### 3.10.3 SPI Timing

Table 23 and Figure 13 through Figure 16 describe the timing requirements for the SPI system.

**Table 23. SPI Timing**

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	$f_{op}$	$f_{BUS}/2048$ 0	$f_{BUS}/2$ $f_{BUS}/4$	Hz
①	D	SPSCK period Master Slave	$t_{SPSCK}$	2 4	2048 —	$t_{cyc}$ $t_{cyc}$
②	D	Enable lead time Master Slave	$t_{Lead}$	1/2 1	— —	$t_{SPSCK}$ $t_{cyc}$
③	D	Enable lag time Master Slave	$t_{Lag}$	1/2 1	— —	$t_{SPSCK}$ $t_{cyc}$
④	D	Clock (SPSCK) high or low time Master Slave	$t_{WSPSCK}$	$t_{cyc} - 30$ $t_{cyc} - 30$	$1024 t_{cyc}$ —	ns ns
⑤	D	Data setup time (inputs) Master Slave	$t_{SU}$	15 15	— —	ns ns
⑥	D	Data hold time (inputs) Master Slave	$t_{HI}$	0 25	— —	ns ns
⑦	D	Slave access time	$t_a$	—	1	$t_{cyc}$
⑧	D	Slave MISO disable time	$t_{dis}$	—	1	$t_{cyc}$
⑨	D	Data valid (after SPSCK edge) Master Slave	$t_v$	— —	25 25	ns ns
⑩	D	Data hold time (outputs) Master Slave	$t_{HO}$	0 0	— —	ns ns
⑪	D	Rise time Input Output	$t_{RI}$ $t_{RO}$	— —	$t_{cyc} - 25$ 25	ns ns
⑫	D	Fall time Input Output	$t_{FI}$ $t_{FO}$	— —	$t_{cyc} - 25$ 25	ns ns

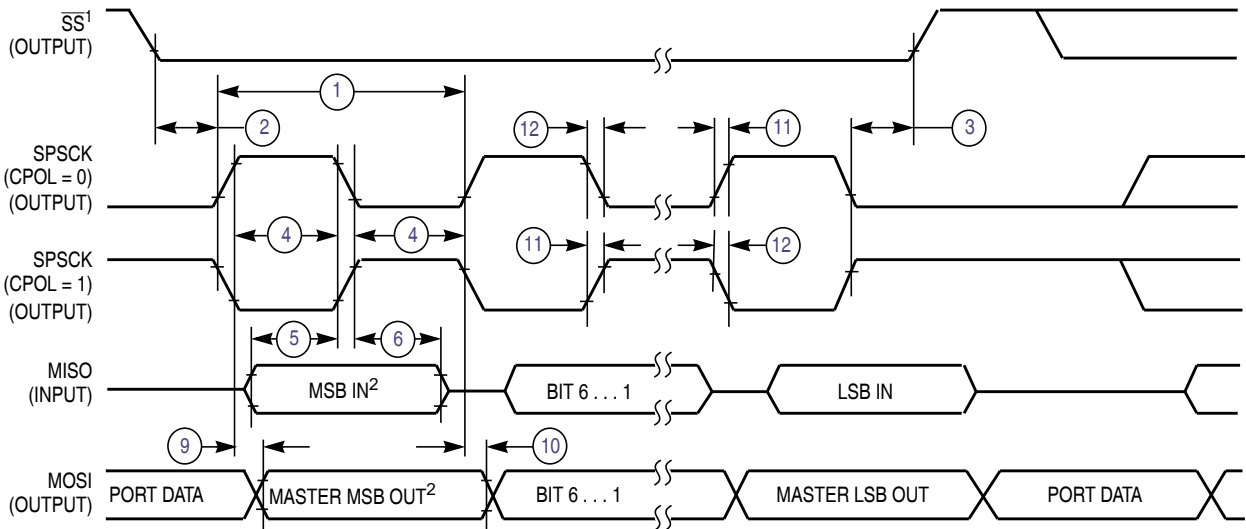
## Electrical Characteristics



### NOTES:

1.  $\overline{SS}$  output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

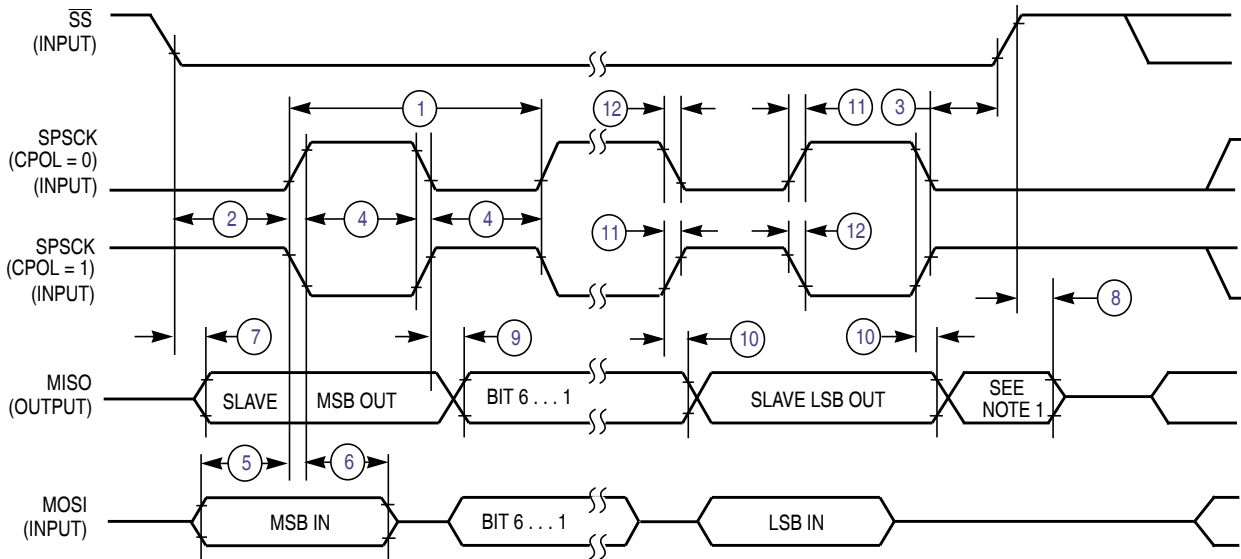
**Figure 13. SPI Master Timing (CPHA = 0)**



### NOTES:

1.  $\overline{SS}$  output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

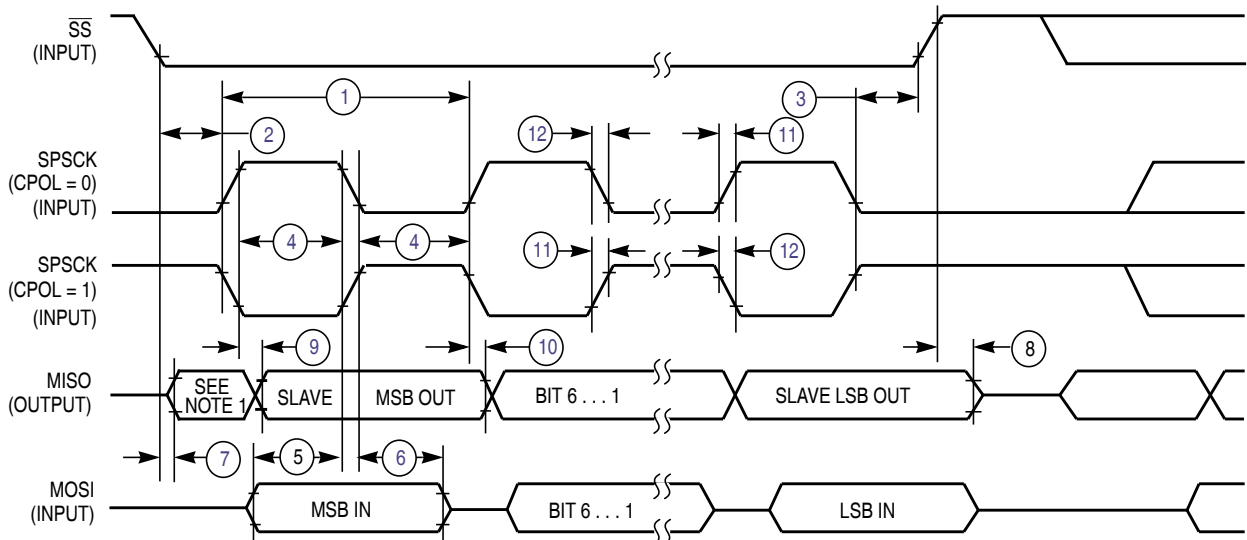
**Figure 14. SPI Master Timing (CPHA = 1)**



NOTE:

1. Not defined but normally MSB of character just received.

Figure 15. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received.

Figure 16. SPI Slave Timing (CPHA = 1)

### 3.11 Analog Comparator (ACMP) Electricals

Table 24. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	$V_{DD}$	1.8	—	3.6	V
C	Supply current (active)	$I_{DDAC}$	—	20	35	$\mu\text{A}$
D	Analog input voltage	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DD}$	V
P	Analog input offset voltage	$V_{AIO}$		20	40	mV
C	Analog comparator hysteresis	$V_H$	3.0	9.0	15.0	mV
P	Analog input leakage current	$I_{ALKG}$	—	—	1.0	$\mu\text{A}$
C	Analog comparator initialization delay	$t_{AINIT}$	—	—	1.0	$\mu\text{s}$

### 3.12 ADC Characteristics

Table 25. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDAD}$	1.8	—	3.6	V	
	Delta to $V_{DD}$ ( $V_{DD} - V_{DDAD}$ ) <sup>2</sup>	$\Delta V_{DDAD}$	-100	0	+100	mV	
Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSAD}$ ) <sup>2</sup>	$\Delta V_{SSAD}$	-100	0	+100	mV	
Ref Voltage High		$V_{REFH}$	1.8	$V_{DDAD}$	$V_{DDAD}$	V	
Input Voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	
Input Capacitance		$C_{ADIN}$	—	4.5	5.5	pF	
Input Resistance		$R_{ADIN}$	—	5	7	k $\Omega$	
Analog Source Resistance	12 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	$R_{AS}$	—	—	2	k $\Omega$	External to MCU
	10 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		—	—	5		
	8 bit mode (all valid $f_{ADCK}$ )		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC=0)	$f_{ADCK}$	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

<sup>1</sup> Typical values assume  $V_{DDAD} = 3.0\text{V}$ , Temp = 25°C,  $f_{ADCK} = 1.0\text{MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> DC potential difference.

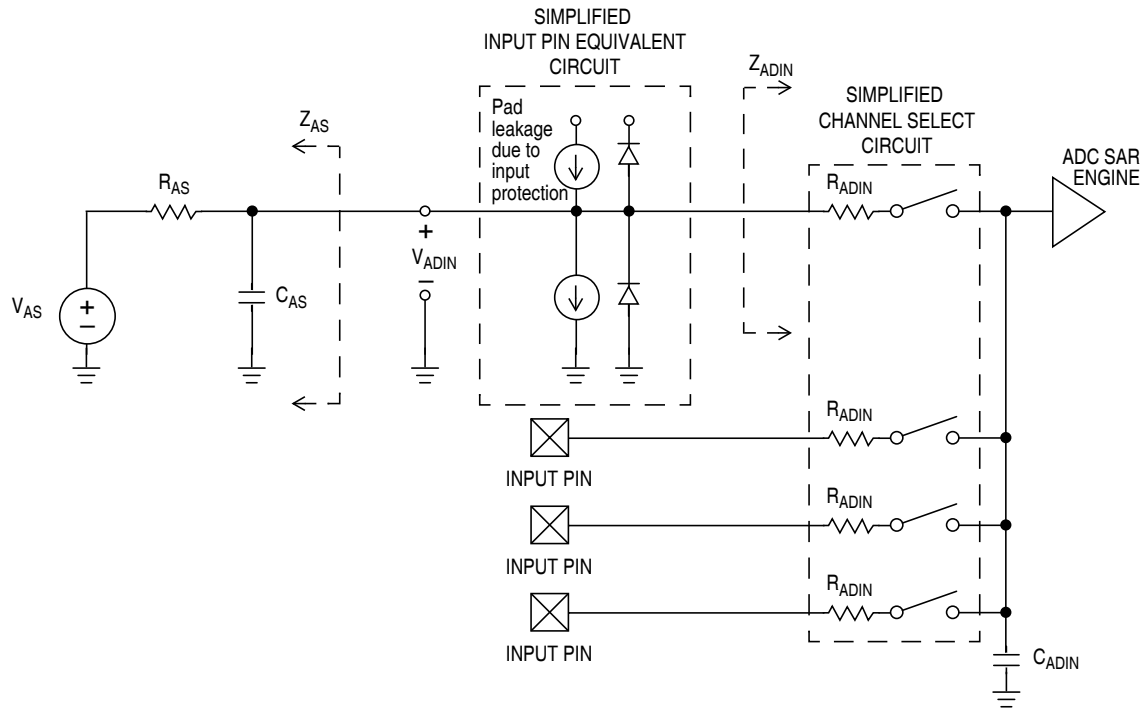


Figure 17. ADC Input Impedance Equivalency Diagram

## Electrical Characteristics

**Table 26. 12-bit ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ )**

C	Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
T	Supply Current ADLPC=1 ADLSMP=1 ADCO=1		$I_{DDAD}$	—	120	—	$\mu\text{A}$	
T	Supply Current ADLPC=1 ADLSMP=0 ADCO=1		$I_{DDAD}$	—	200	—	$\mu\text{A}$	
T	Supply Current ADLPC=0 ADLSMP=1 ADCO=1		$I_{DDAD}$	—	290	—	$\mu\text{A}$	
P	Supply Current ADLPC=0 ADLSMP=0 ADCO=1		$I_{DDAD}$	—	0.53	1	mA	
P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	$f_{ADACK}$	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
C		Low Power (ADLPC=1)		1.25	2	3.3		
P	Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	$t_{ADC}$	—	20	—	ADCK cycles	See ADC chapter in the LL16 Reference Manual for conversion time variances
C		Long Sample (ADLSMP=1)		—	40	—		
P	Sample Time	Short Sample (ADLSMP=0)	$t_{ADS}$	—	3.5	—	ADCK cycles	
C		Long Sample (ADLSMP=1)		—	23.5	—		
T	Total Unadjusted Error	12 bit mode	$E_{TUE}$	—	$\pm 3.0$	—	$\text{LSB}^2$	
P		10 bit mode		—	$\pm 1$	$\pm 2.5$		
T		8 bit mode		—	$\pm 0.5$	$\pm 1.0$		
T	Differential Non-Linearity	12 bit mode	DNL	—	$\pm 1.75$	—	$\text{LSB}^2$	
P		10 bit mode <sup>3</sup>		—	$\pm 0.5$	$\pm 1.0$		
T		8 bit mode <sup>3</sup>		—	$\pm 0.3$	$\pm 0.5$		
T	Integral Non-Linearity	12 bit mode	INL	—	$\pm 1.5$	—	$\text{LSB}^2$	
P		10 bit mode		—	$\pm 0.5$	$\pm 1.0$		
T		8 bit mode		—	$\pm 0.3$	$\pm 0.5$		
T	Zero-Scale Error	12 bit mode	$E_{ZS}$	—	$\pm 1.5$	—	$\text{LSB}^2$	$V_{ADIN} = V_{SSAD}$
P		10 bit mode		—	$\pm 0.5$	$\pm 1.5$		
T		8 bit mode		—	$\pm 0.5$	$\pm 0.5$		

Table 26. 12-bit ADC Characteristics ( $V_{REFH} = V_{DDAD}$ ,  $V_{REFL} = V_{SSAD}$ ) (continued)

C	Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
T	Full-Scale Error	12 bit mode	$E_{FS}$	—	±1.0	—	LSB <sup>2</sup>	$V_{ADIN} = V_{DDAD}$
P		10 bit mode		—	±0.5	±1		
T		8 bit mode		—	±0.5	±0.5		
D	Quantization Error	12 bit mode	$E_Q$	—	-1 to 0	—	LSB <sup>2</sup>	
		10 bit mode		—	—	±0.5		
		8 bit mode		—	—	±0.5		
D	Input Leakage Error	12 bit mode	$E_{IL}$	—	±2	—	LSB <sup>2</sup>	Pad leakage <sup>4*</sup> $R_{AS}$
		10 bit mode		—	±0.2	±4		
		8 bit mode		—	±0.1	±1.2		
D	Temp Sensor Slope	-40°C to 25°C	m	—	1.646	—	mV/ C	
		25°C to 85°C		—	1.769	—		
D	Temp Sensor Voltage	25°C	$V_{TEMP25}$	—	701.2	—	mV	

<sup>1</sup> Typical values assume  $V_{DDAD} = 3.0V$ , Temp = 25°C,  $f_{ADCK} = 1.0MHz$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup>  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$

<sup>3</sup> Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

<sup>4</sup> Based on input pad leakage current. Refer to pad electricals.

### 3.13 LCD Specifications

Table 27. LCD Electricals, 3-V Glass

C	Characteristic	Symbol	Min	Typ	Max	Unit
D	LCD Supply Voltage	$V_{LCD}$	.9	1.5	1.8	V
D	LCD Frame Frequency	$f_{Frame}$	28	30	58	Hz
D	LCD Charge Pump Capacitance	$C_{LCD}$		100	100	nF
D	LCD Bypass Capacitance	$C_{BYLCD}$		100	100	nF
D	LCD Glass Capacitance	$C_{glass}$		2000	8000	pF
D	$V_{IREG}$	HRefSel = 0 HRefSel = 1	.89 1.49	1.00 1.67	1.15 1.85 <sup>1</sup>	V
D	$V_{IREG}$ TRIM Resolution	$\Delta_{RTRIM}$	1.5			% $V_{IREG}$
D	$V_{IREG}$ Ripple	HRefSel = 0 HRefSel = 1			.1 .15	V
D	$V_{LCD}$ Buffered Adder <sup>2</sup>	$I_{Buff}$		1		$\mu A$

<sup>1</sup>  $V_{IREG}$  Max can not exceed  $V_{DD} - 0.15$  V

<sup>2</sup>  $V_{SUPPLY} = 10$ ,  $BYPASS = 0$

### 3.14 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory.

Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply. For more detailed information about program/erase operations, see the Memory section.



## 3.15 EMC Performance

Table 28. FLASH Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{\text{prog/erase}}$	1.8		3.6	V
D	Supply voltage for read operation	$V_{\text{Read}}$	1.8		3.6	V
D	Internal FCLK frequency <sup>1</sup>	$f_{\text{FCLK}}$	150		200	kHz
D	Internal FCLK period (1/FCLK)	$t_{\text{FcyC}}$	5		6.67	μs
P	Byte program time (random location) <sup>2</sup>	$t_{\text{prog}}$		9		$t_{\text{FcyC}}$
P	Byte program time (burst mode) <sup>2</sup>	$t_{\text{Burst}}$		4		$t_{\text{FcyC}}$
P	Page erase time <sup>2</sup>	$t_{\text{Page}}$		4000		$t_{\text{FcyC}}$
P	Mass erase time <sup>2</sup>	$t_{\text{Mass}}$		20,000		$t_{\text{FcyC}}$
D	Byte program current <sup>3</sup>	$R_{\text{IDDBP}}$	—	4	—	mA
D	Page erase current <sup>3</sup>	$R_{\text{IDDPPE}}$	—	6	—	mA
C	Program/erase endurance <sup>4</sup> $T_L$ to $T_H = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $T = 25^\circ\text{C}$		10,000	— 100,000	— —	cycles
C	Data retention <sup>5</sup>	$t_{\text{D\_ret}}$	15	100	—	years

<sup>1</sup> The frequency of this clock is controlled by a software setting.

<sup>2</sup> These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

<sup>3</sup> The program and erase currents are additional to the standard run  $I_{\text{DD}}$ . These values are measured at room temperatures with  $V_{\text{DD}} = 3.0$  V, bus frequency = 4.0 MHz.

<sup>4</sup> Typical endurance for FLASH was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

<sup>5</sup> Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

### 3.15.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

## Ordering Information

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

**Table 29. Radiated Emissions, Electric Field**

Parameter	Symbol	Conditions	Frequency	$f_{osc}/f_{BUS}$	Level <sup>1</sup> (Max)	Unit	
Radiated emissions, electric field	$V_{RE\_TEM}$	$V_{DD} = 3.3\text{ V}$ $T_A = +25^\circ\text{C}$ package type 64-pin LQFP	0.15 – 50 MHz	32 kHz crystal 10 MHz bus	-7	dB $\mu$ V	
			50 – 150 MHz		-9		
			150 – 500 MHz		-6		
			500 – 1000 MHz		-6		
			IEC Level		N		—
			SAE Level		1		—

<sup>1</sup> Data based on qualification test results.

The susceptibility performance classification is described in [Table 30](#).

**Table 30. Susceptibility Performance Classification**

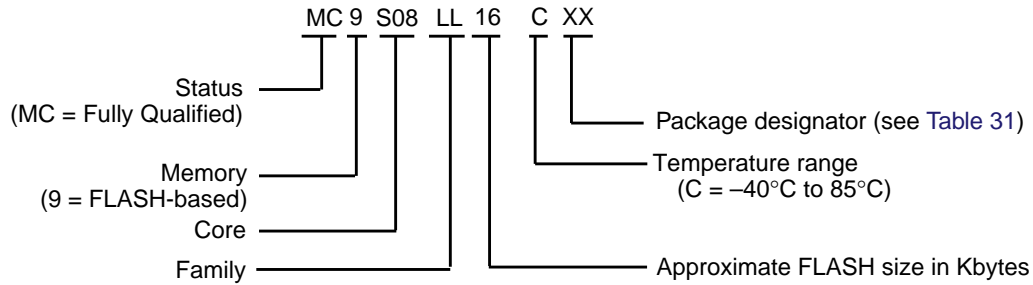
Result	Performance Criteria	
A	No failure	The MCU performs as designed during and after exposure.
B	Self-recovering failure	The MCU does not perform as designed during exposure. The MCU returns automatically to normal operation after exposure is removed.
C	Soft failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the RESET pin is asserted.
D	Hard failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the power to the MCU is cycled.
E	Damage	The MCU does not perform as designed during and after exposure. The MCU cannot be returned to proper operation due to physical damage or other permanent performance degradation.

## 4 Ordering Information

This section contains the ordering information and the device numbering system for the MC9S08LL16 Series.

## 4.1 Device Numbering System

Example of the device numbering system:



## 5 Package Information and Mechanical Drawings

Table 31 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08LL16 Series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in Table 31, or
- Open a browser to the Freescale® website (<http://www.freescale.com>), and enter the appropriate document number (from Table 31) in the “Enter Keyword” search box at the top of the page.

**Table 31. Package Descriptions**

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
64	Low Quad Flat Package	LQFP	LH	840F	<a href="#">98ASS23234W</a>
48	Low Quad Flat Package	LQFP	LF	932	<a href="#">98ASH00962A</a>
48	Quad Flat No-Leads	QFN	GT	1314	<a href="#">98ARH99048A</a>

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